High Side & Low Side Gate Driver

General Description

The ID7186 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600V. Propagation delays are matched to simplify use in high frequency applications.

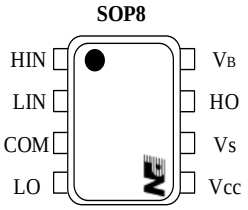
Application

- Major home appliance
- Drives
- EV charging
- Motor inverter

Features

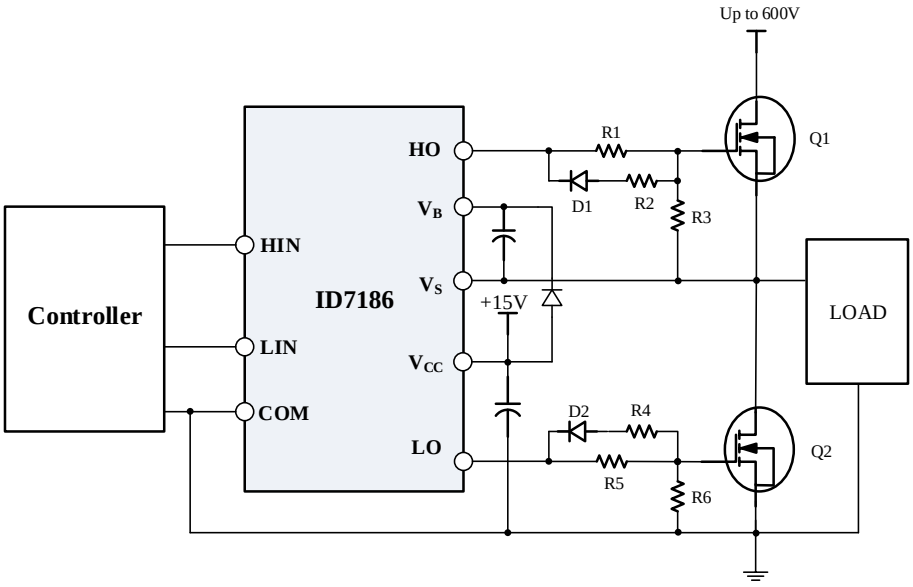
- Fully operational to +600V
- 3.3V and 5V logic compatible
- Floating channel designed for bootstrap operation
- Gate drive supply range from 10V to 20V
- Matched propagation delay for both channels
- UVLO for both channels
- Tolerant to negative transient voltage
- dV/dt immune
- 4A/4A output current capability

Package/Order Information



Order code	Package
ID7186SEC-R1	SOP8

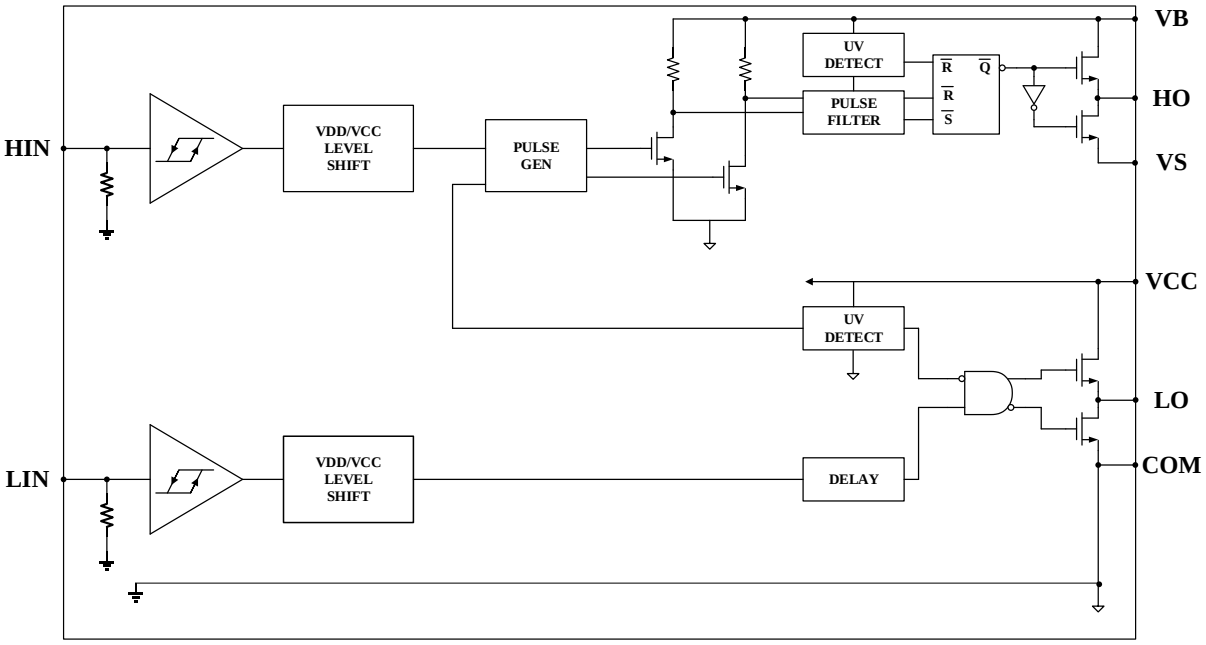
Typical Application



Pin Definitions

Pin Name	Pin Number	Pin Function Description
HIN	1	Logic input for high side gate driver output (HO), in phase
LIN	2	Logic input for low side gate driver output (LO), in phase
COM	3	Low side return
LO	4	Low side gate drive output
VCC	5	Low side supply
VS	6	High side floating supply return
HO	7	High side gate drive output
VB	8	High side floating supply

Block Diagram



Absolute Maximum Ratings

Exceeding these ratings may damage the device.
The absolute maximum ratings are stress ratings only at T_A=25 ℃, unless otherwise specified.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply voltage	-0.3	620	V
V_S	High side floating supply offset voltage	V_B - 20	V_B + 0.3	
V_{HO}	High side gate drive output voltage	V_S -0.3	V_B + 0.3	
VCC	Low side supply voltage	-0.3	20	
V_{LO}	Low side gate drive output voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN, LIN)	V_{SS}-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	--	50	V/ns
ESD	HBM Model	2	--	kV
	CDM Model	200	--	V
P_D	Package Power Dissipation @ T_A ≤25°C	--	1.25	W
R_{thJA}	Thermal Resistance Junction to Ambient	--	120	℃ /W
T_J	Junction Temperature	--	150	℃
T_S	Storage Temperature	-50	150	
T_L	Lead Temperature (Soldering, 10 seconds)	--	300	

Recommended Operating Conditions

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S +10	V_S +20	V
V_S	High side floating supply offset voltage	--	600	
V_{HO}	High side gate floating output voltage	V_S	V_B	
VCC	Low side fixed supply voltage	10	20	
V_{LO}	Low side output voltage	GND	VCC	
V_{IN}	Logic input voltage(HIN & LIN)	GND	VCC	
T_A	Ambient temperature	-40	125	℃

Dynamic Electrical Characteristics

(V_{BIAS} (VCC, V_{BS}) = 15V, C_L = 1000pF and T_A = 25℃ unless otherwise specified.)

Symbol	Definition	Test Condition	MIN.	TYP.	MAX.	Units
t_{on_H}	Turn-on propagation delay(HIN to HO)	VS = 0V	-	110	-	ns
t_{off_H}	Turn-off propagation delay(HIN to HO)	VS = 600V	-	110	-	
t_{on_L}	Turn-on propagation delay(LIN to LO)	VS = 0V	-	60	-	
t_{off_L}	Turn-off propagation delay(LIN to LO)	VS = 0V	-	60	-	
t_r	Turn-on rise time		-	18	-	
t_f	Turn-off fall time		-	12	-	
MT	Dealy matching, HS&LS turn on/off		-	-	70	

Static Electrical Characteristics

(V_{BIAS} (VCC, V_{BS}) = 15V, C_L = 1000pF and T_A = 25℃ unless otherwise specified.)

Symbol	Definition	Test Condition	MIN.	TYP.	MAX.	Units
V_{IH}	Logic “1”(HIN& LIN) input voltage		2.6	-	-	V
V_{IL}	Logic “0” (HIN & LIN) input voltage		-	-	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O=20mA	-	0.2	0.4	
V_{OL}	Low level output voltage, V_O		-	-	0.15	
I_{QCC}	Quiescent VCC supply current	V_{IN} = 0V	-	100	200	μA
I_{QCC}	Quiescent VCC supply current	V_{IN} = 5V	-	120	240	
I_{QBS}	Quiescent V_{BS} supply current	V_{IN} = 0V	-	95	190	
I_{QBS}	Quiescent V_{BS} supply current	V_{IN} = 5V	-	130	240	
I_{LK}	Leakage current from VS(600V) to GND	V_B = V_S = 600V	-	-	10	
I_{IN+}	Logic “1” input bias current	V_{IN} = VCC	-	25	60	
I_{IN-}	Logic “0” input bias current	V_{IN} = 0V	-	-	5	
V_{BSU+}	V_{BS} supply UVLO threshold		8.4	9.2	10	V
V_{BSU-}			7.6	8.4	9.2	
V_{CCU+}	VCC supply UVLO threshold		8.4	9.2	10	
V_{CCU-}			7.6	8.4	9.2	
I_{O+}	Output high short circuit pulsed current	V_O = 0V, V_{IN} = VCC PW ≤ 10us	3.5	4	-	A
I_{O-}	Output low short circuit pulsed current	V_O = 15V, V_{IN} = 0V PW ≤ 10us	3.5	4	-	

Function Timing Diagram

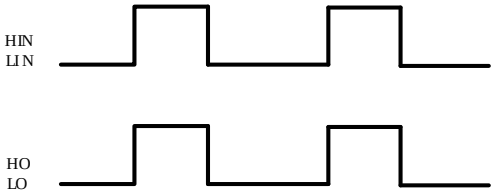


Fig.1 Input and output logic

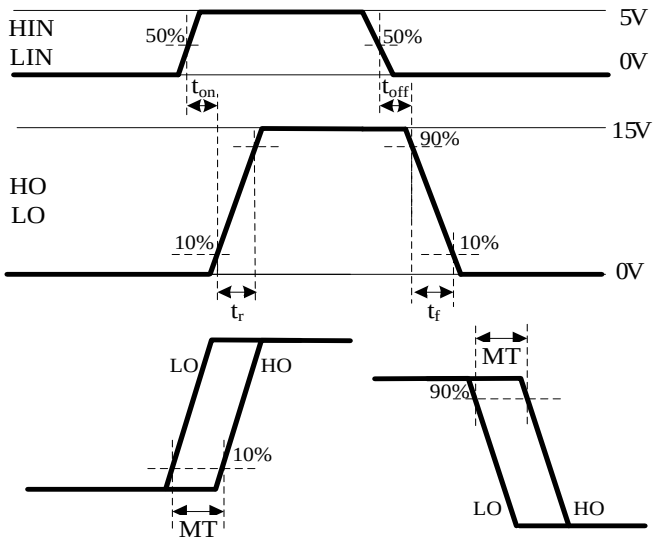


Fig.2 Propagation Delay, Rise Time, Fall Time Timing and Delay Matching

Typical Characteristics Plots

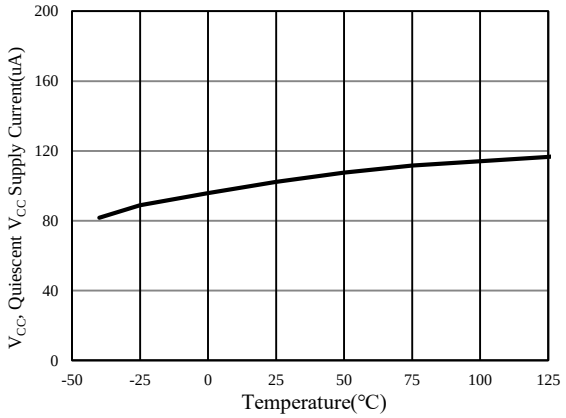


Figure 3. Quiescent V_{CC} Supply Current vs. Temperature

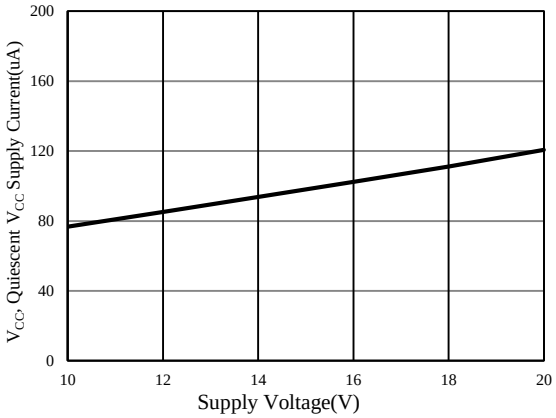


Figure 4. Quiescent V_{CC} supply current vs. Supply Voltage

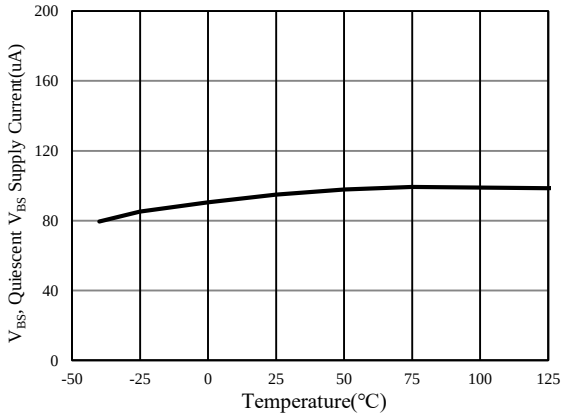


Figure 5. Quiescent V_{BS} Supply Current vs. Temperature

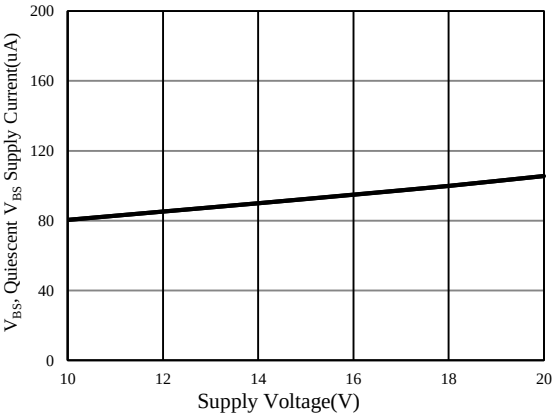


Figure 6. Quiescent V_{BS} supply current vs. Supply Voltage

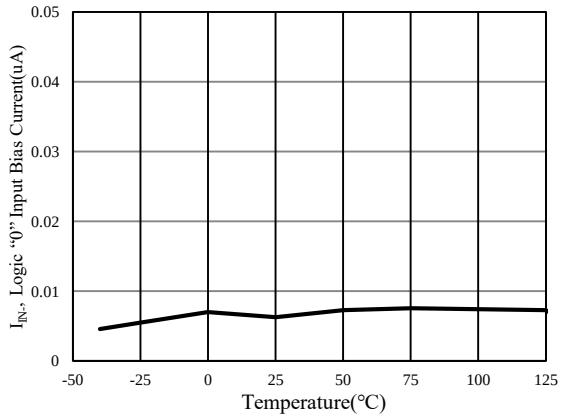


Figure 7. Logic "0" Input Bias Current vs. Temperature

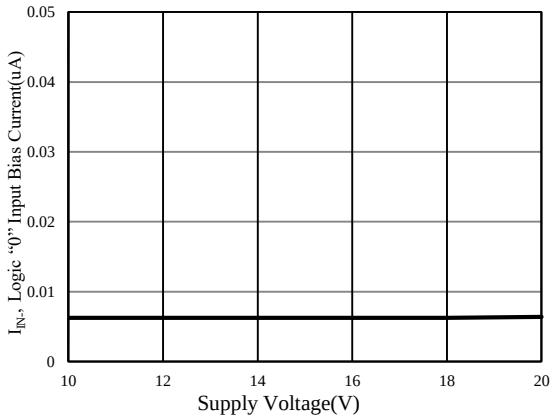


Figure 8. Logic "0" Input Bias Current vs. Supply Voltage

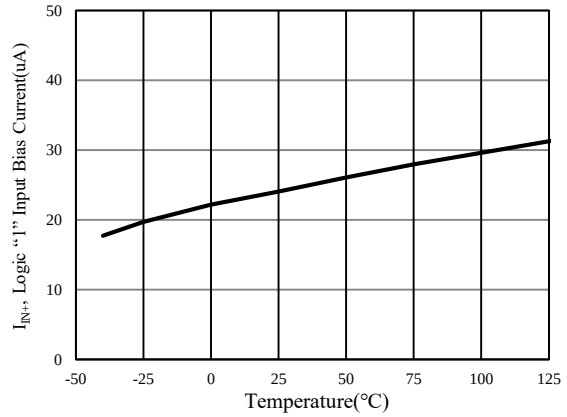


Figure 9. Logic "1" Input Bias Current vs. Temperature

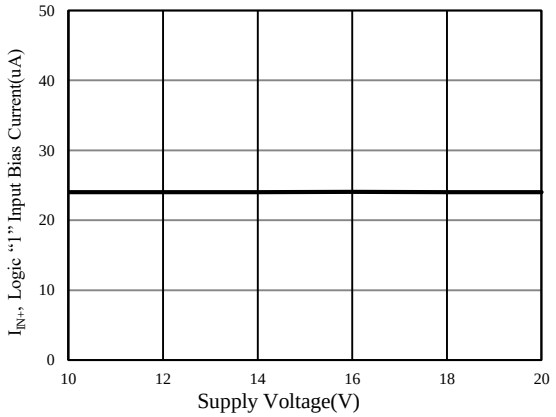


Figure 10. Logic "1" Input Bias Current vs. Supply Voltage

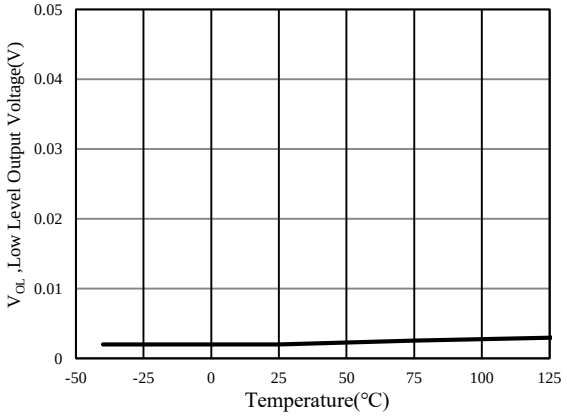


Figure 11. Low Level Output Voltage(I_O=2mA) vs. Temperature

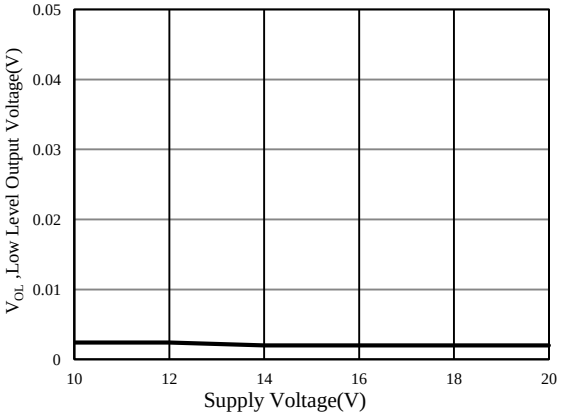


Figure 12. Low Level Output Voltage(I_O=2mA) vs. Supply Voltage

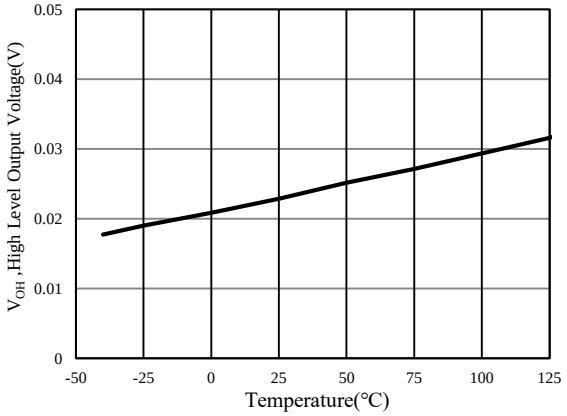


Figure 13. High Level Output Voltage(I_O=2mA) vs. Temperature

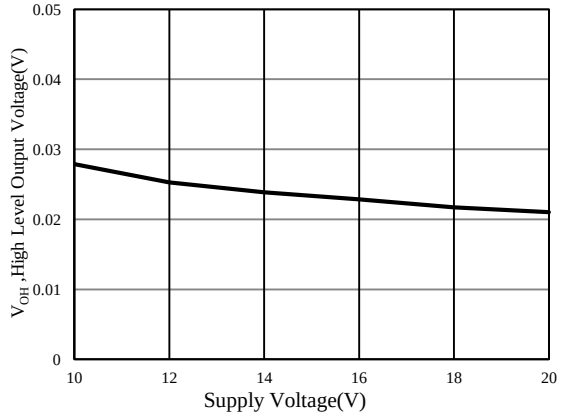


Figure 14. High Level Output Voltage(I_O=2mA) vs. Supply Voltage

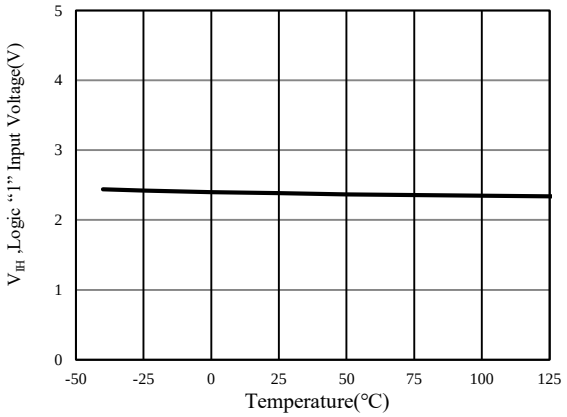


Figure 15. Logic "1" input voltage vs. Temperature

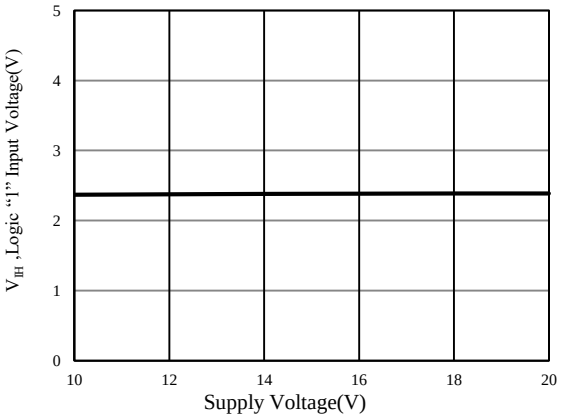


Figure 16. Logic "1" input voltage vs. Supply Voltage

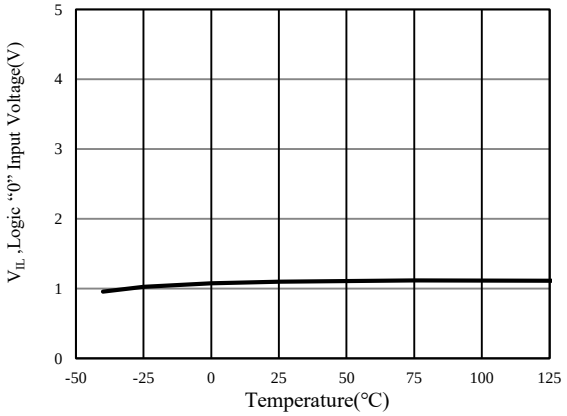


Figure 17. Logic "0" input voltage vs. Temperature

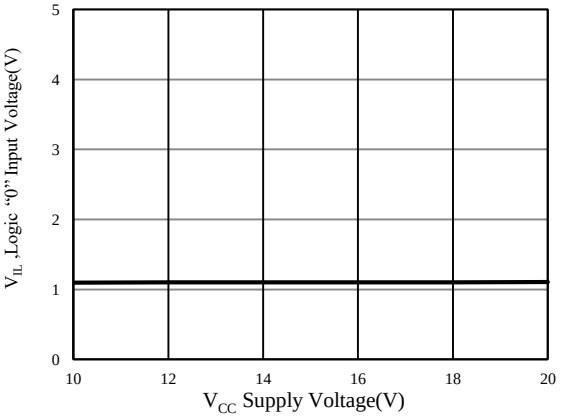


Figure 18. Logic "0" input voltage vs. Supply Voltage

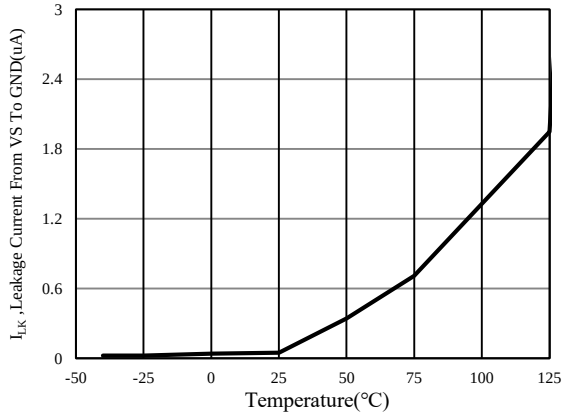


Figure 19. Leakage Current From VS(600V) To GND vs. Temperature

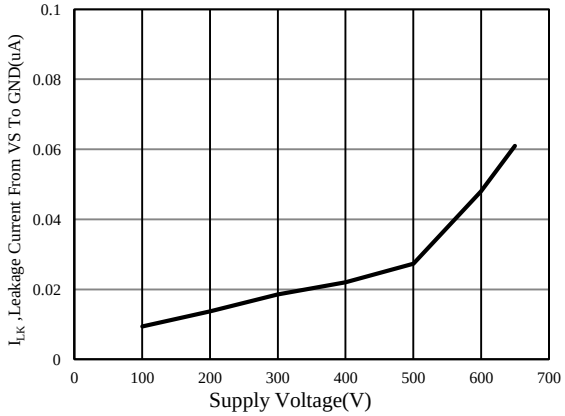


Figure 20. Leakage Current From VS To GND vs. Supply Voltage

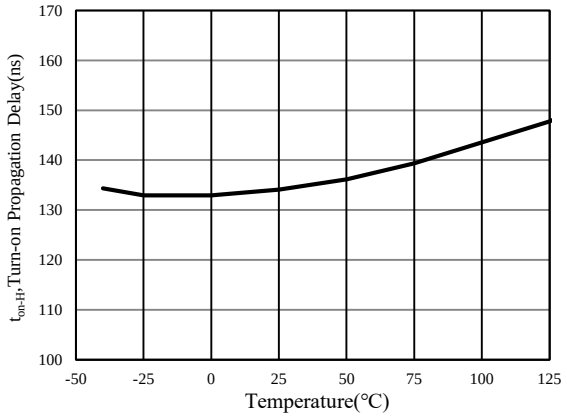


Figure 21. Turn-on Propagation Delay(HIN to HO) vs. Temperature

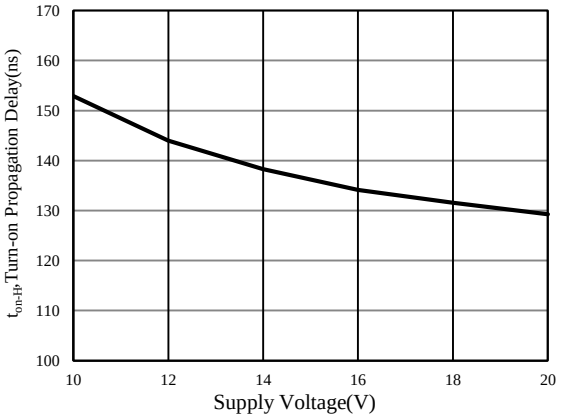


Figure 22. Turn-on Propagation Delay(HIN to HO) vs. Supply Voltage

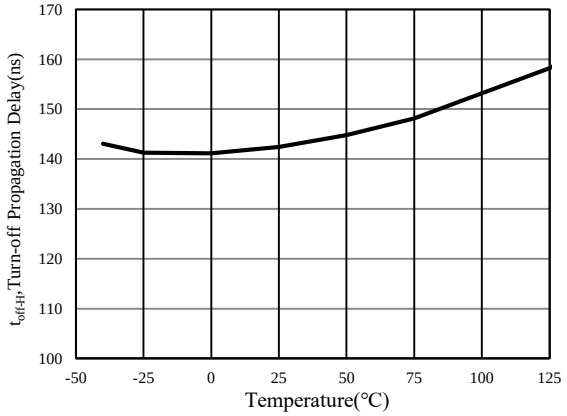


Figure 23. Turn-off Propagation Delay(HIN to HO) vs. Temperature

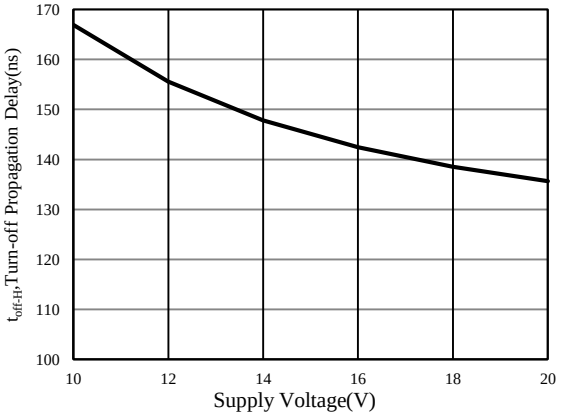


Figure 24. Turn-off Propagation Delay(HIN to HO) vs. Supply Voltage

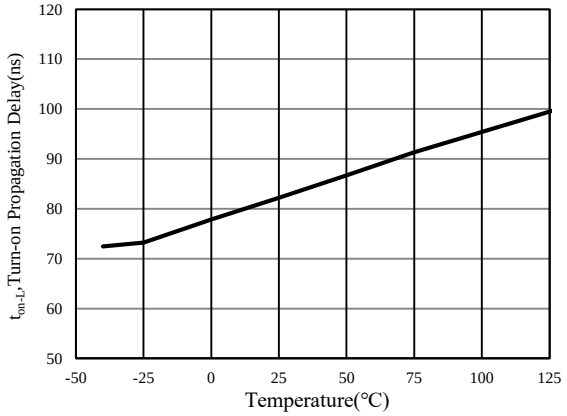


Figure 25. Turn-on Propagation Delay(LIN to LO) vs. Temperature

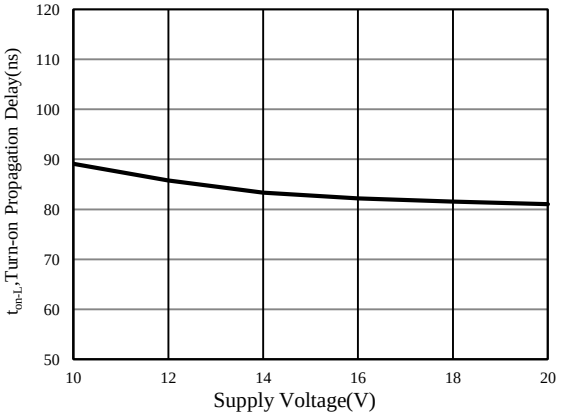


Figure 26. Turn-on Propagation Delay(LIN to LO) vs. Supply Voltage

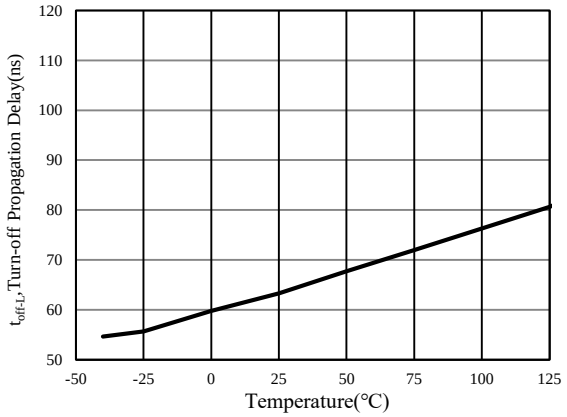


Figure 27. Turn-off Propagation Delay(LIN to LO) vs. Temperature

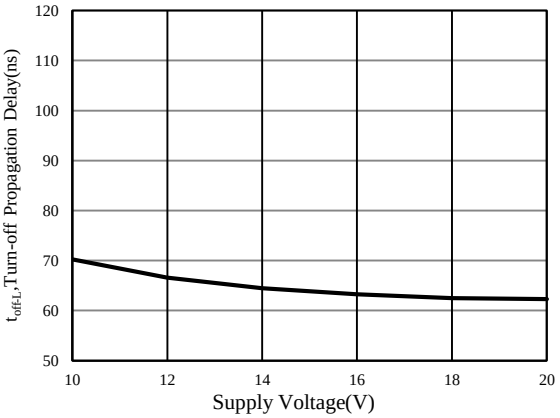


Figure 28. Turn-off Propagation Delay(LIN to LO) vs. Supply Voltage

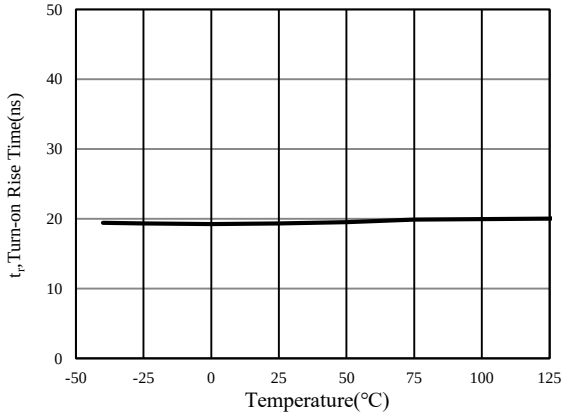


Figure 29. Turn-on Rise Time vs. Temperature

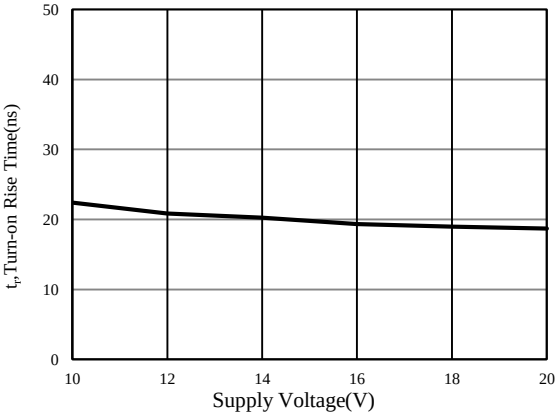


Figure 30. Turn-on Rise Time vs. Supply Voltage

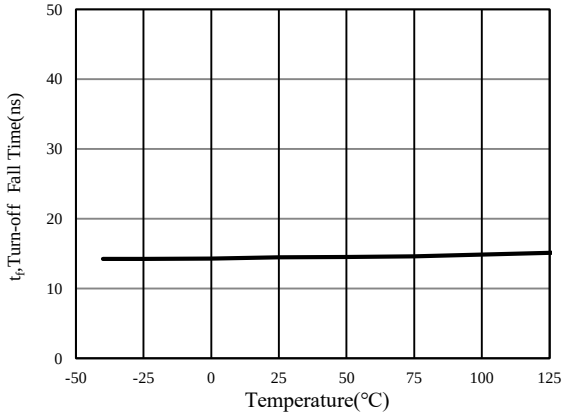


Figure 31. Turn-off Fall Time vs. Temperature

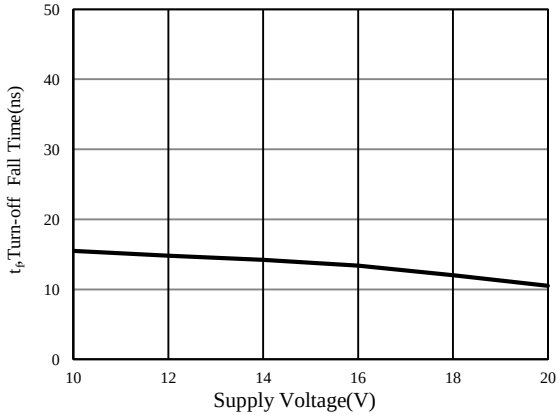


Figure 32. Turn-off Fall Time vs. Supply Voltage

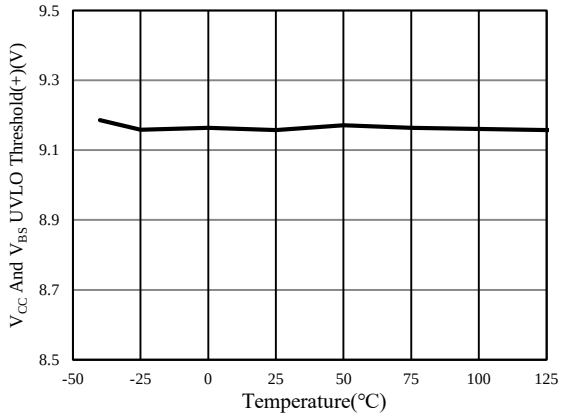


Figure 33. V_{CC} And V_{BS} UVLO Threshold(+) vs. Temperature

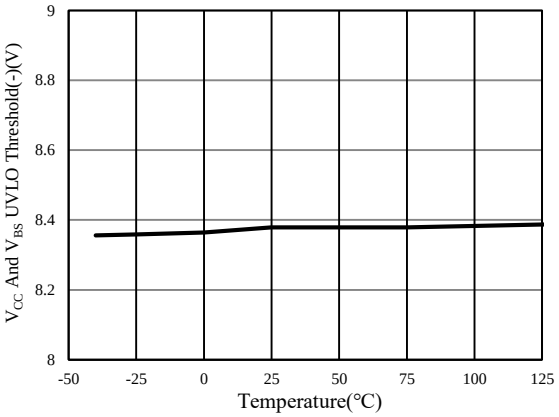
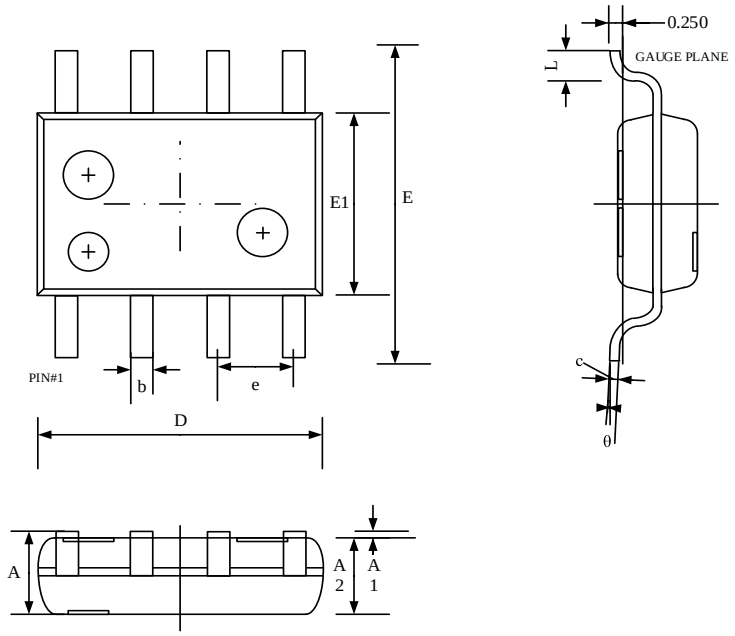


Figure 34. V_{CC} And V_{BS} UVLO Threshold(-) vs. Temperature

Package Information

Package Information SOP8



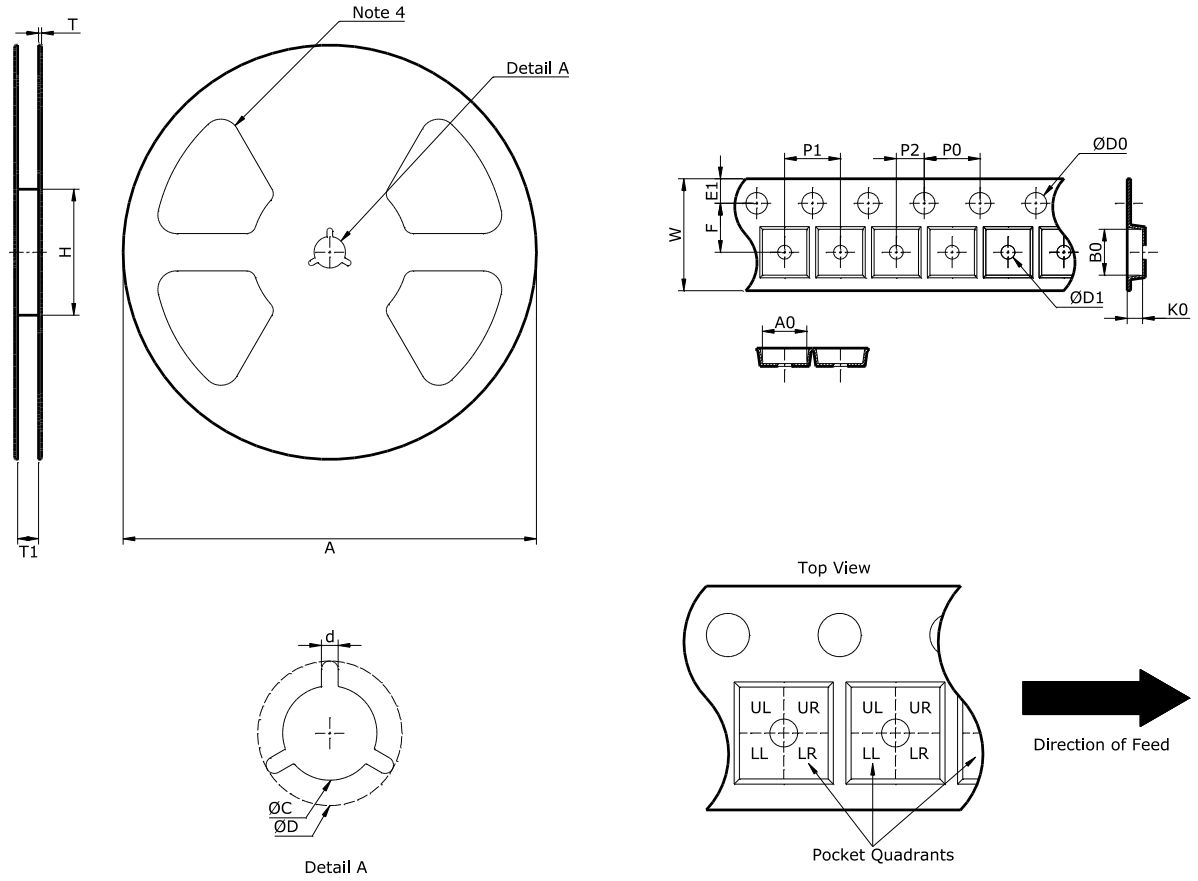
Size / Symbol	Min. (mm)	Max. (mm)	Size / Symbol	Min. (mm)	Max. (mm)
A	1.300	1.750	E	5.800	6.25
A1	0.000	0.250	E1	3.750	4.150
A2	1.250	1.600	e	1.27	
b	0.306	0.510	L	0.400	1.270
c	0.150	0.250	θ	0 °	12 °
D	4.700	5.100			

Top mark	Package
iDR. ID7186 YWWXXXXX	SOP8

Note：Y：Year Code；WW：Week Code；XXXXX：Internal Code

Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

Tape and Reel Information



SOP8 Package								
A (mm)	**T (mm)**	**T1 (mm)**	**H (mm)**	**ØC (mm)**	**d (mm)**	**A0 (mm)**	**B0 (mm)**	**K0 (mm)**
330 ±2.0	3max	14 +4.5/-4	100 ±2	13.4 +0.2/-0.6	2.5 ±1	6.60 +0.1/-0.3	5.3 +0.2/-0.1	2 ±0.2
W (mm)	**F (mm)**	**E1 (mm)**	**P0 (mm)**	**P1 (mm)**	**P2 (mm)**	**ØD0 (mm)**	**ØD1 (mm)**	**Pin 1 Quadrant**
12.00 ±0.3	5.50 ±0.1	1.75 ±0.10	4.00 ±0.10	8.0 ±0.1	2.0 ±0.1	1.5 +0.1/-0	1.5 +0.25/-0	UL

Notes:
1. This drawing is subjected to change without notice.
2. All dimensions are nominal and in mm.
3. This drawing is not in scale and for reference only. Customer can contact Chipown sales representative for further details.
4. The number of flange openings depends on the reel size and assembly site. This drawing shows an example only.

Important Notice

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