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# FQB34N20L

## N-Channel QFET® MOSFET

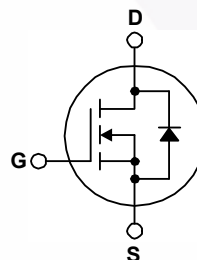
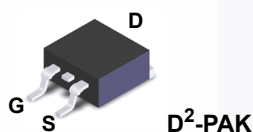
200 V, 31 A, 75 mΩ

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

- 31 A, 200 V,  $R_{DS(on)} = 75 \text{ m}\Omega$  (max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 15.5 \text{ A}$
- Low Gate Charge (Typ. 55 nC)
- Low  $C_{rss}$  (Typ. 52 pF)
- 100% Avalanche Tested
- Low level gate drive requirement allowing direct operation from logic drivers
- RoHS Compliant



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQB34N20LTM	Unit
$V_{DSS}$	Drain-Source Voltage	200	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	31	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	20	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	124	A
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	640	mJ
$I_{AR}$	Avalanche Current (Note 1)	31	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	18	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	3.13	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	180	W
	- Derate above $25^\circ\text{C}$	1.43	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQB34N20LTM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.7	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (* 1 in <sup>2</sup> pad of 2 oz copper), Max.	40	

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQB34N20L	FQB34N20LTM	D2-PAK	330mm	24mm	800

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	200	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.16	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 160\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0	--	2.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 15.5\text{ A}$	--	0.057	0.075	$\Omega$
		$V_{GS} = 5\text{ V}, I_D = 15.5\text{ A}$	--	0.060	0.080	
$g_{FS}$	Forward Transconductance	$V_{DS} = 30\text{ V}, I_D = 15.5\text{ A}$	--	41	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	3000	3900	pF
$C_{oss}$	Output Capacitance		--	400	520	pF
$C_{rss}$	Reverse Transfer Capacitance		--	52	67	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100\text{ V}, I_D = 34\text{ A},$ $R_G = 25\ \Omega$	--	45	100	ns
$t_r$	Turn-On Rise Time		--	520	1050	ns
$t_{d(off)}$	Turn-Off Delay Time		--	170	350	ns
$t_f$	Turn-Off Fall Time		(Note 4)	--	370	750
$Q_g$	Total Gate Charge	$V_{DS} = 160\text{ V}, I_D = 34\text{ A},$ $V_{GS} = 5\text{ V}$	--	55	72	nC
$Q_{gs}$	Gate-Source Charge		--	9.9	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4)	--	27	--

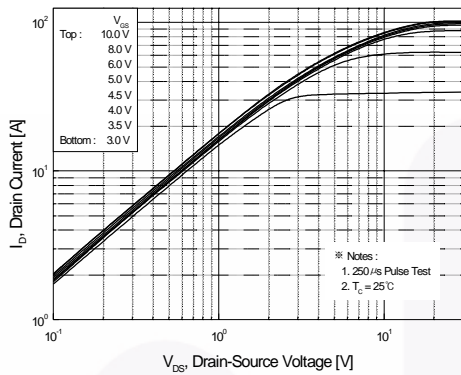
### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	31	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	124	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 31\text{ A}$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 34\text{ A},$	--	205	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$	--	1.1	--	$\mu\text{C}$

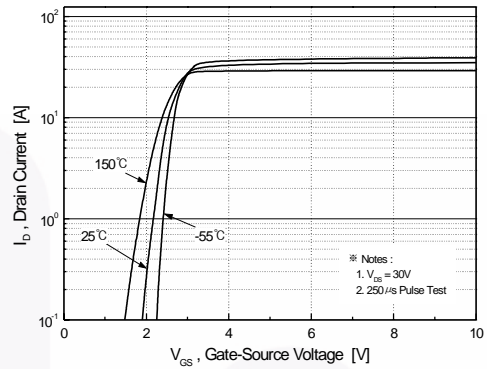
#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 1.0\text{ mH}, I_{AS} = 31\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 34\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature

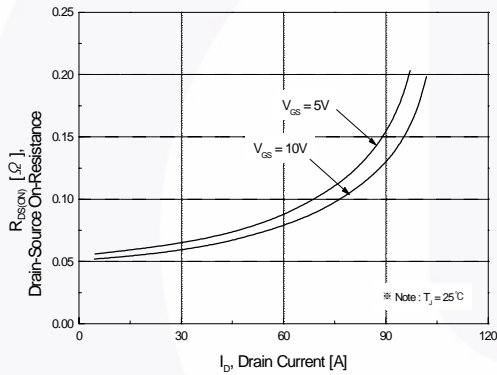
## Typical Characteristics



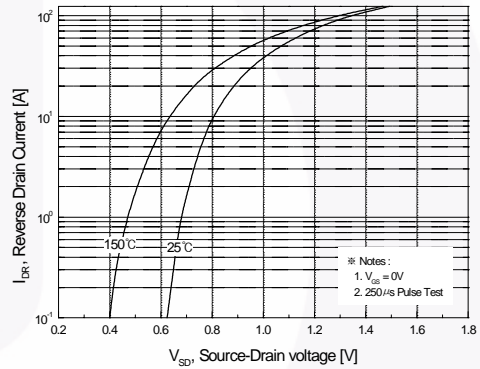
**Figure 1. On-Region Characteristics**



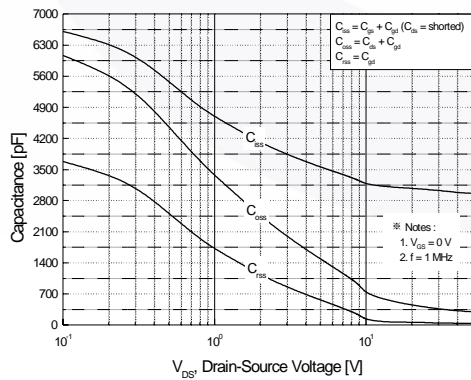
**Figure 2. Transfer Characteristics**



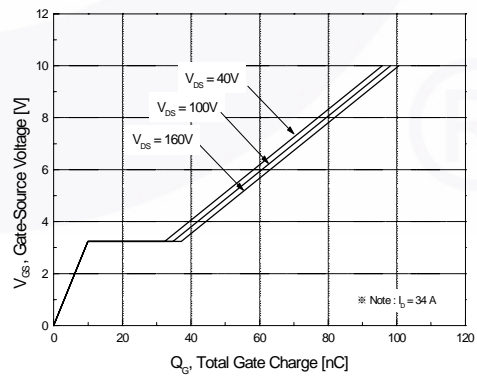
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

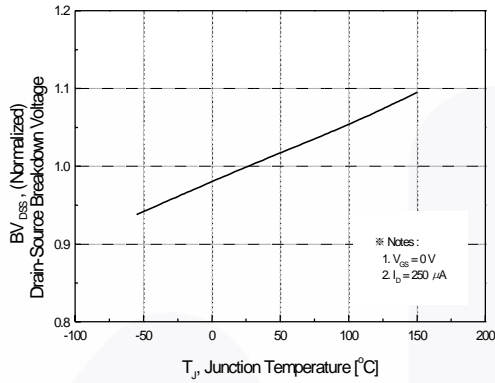


**Figure 5. Capacitance Characteristics**

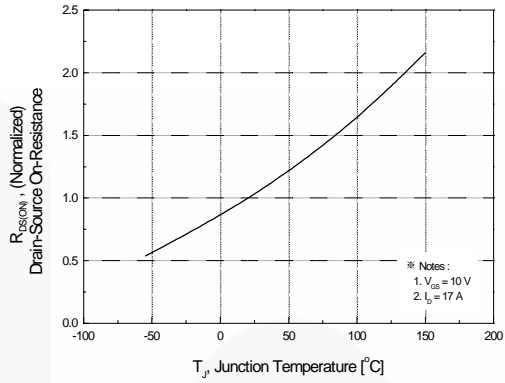


**Figure 6. Gate Charge Characteristics**

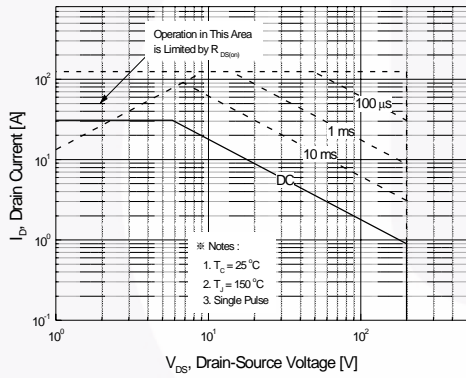
## Typical Characteristics (Continued)



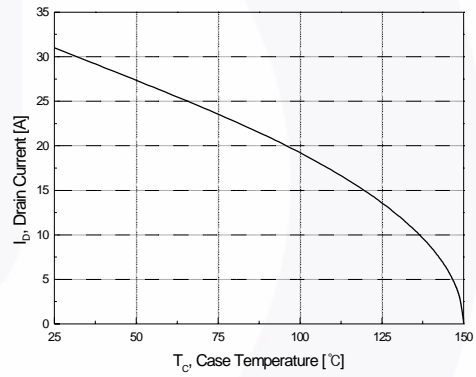
**Figure 7. Breakdown Voltage Variation vs. Temperature**



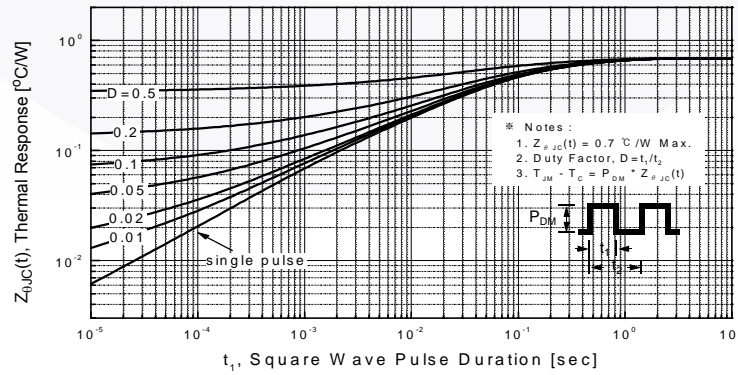
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

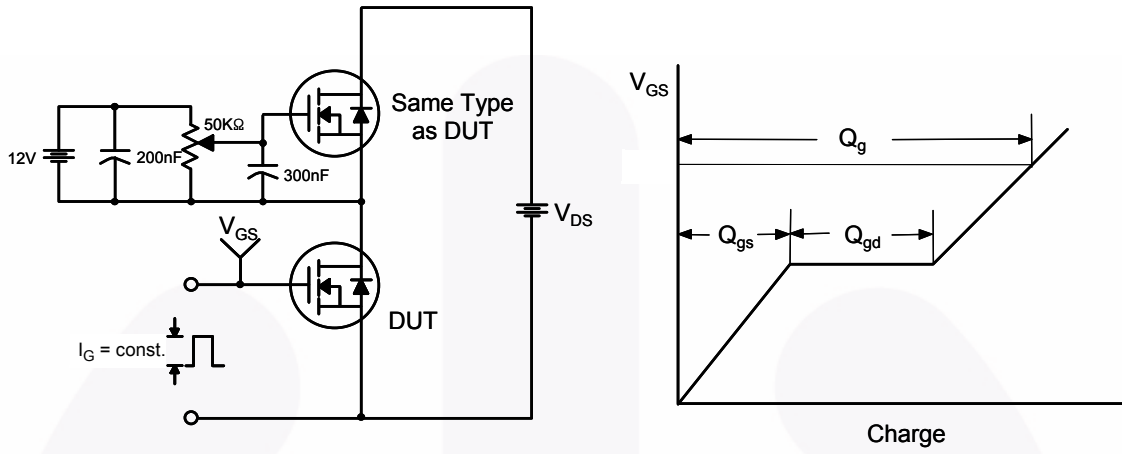


**Figure 10. Maximum Drain Current vs. Case Temperature**

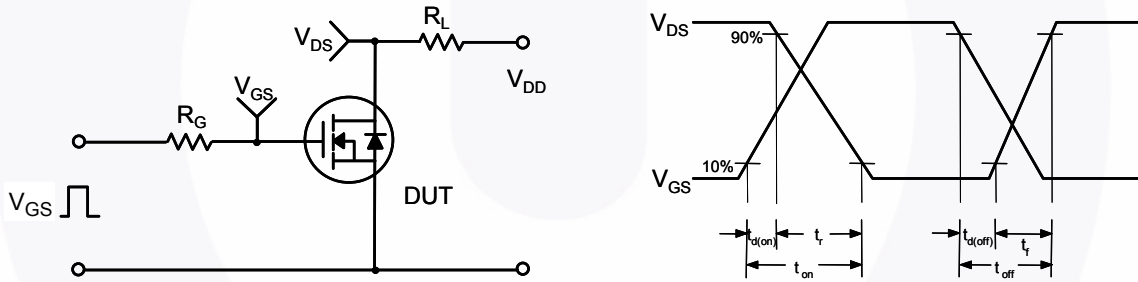


**Figure 11. Transient Thermal Response Curve**

**Figure 12. Gate Charge Test Circuit & Waveform**



**Figure 13. Resistive Switching Test Circuit & Waveforms**



**Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms**

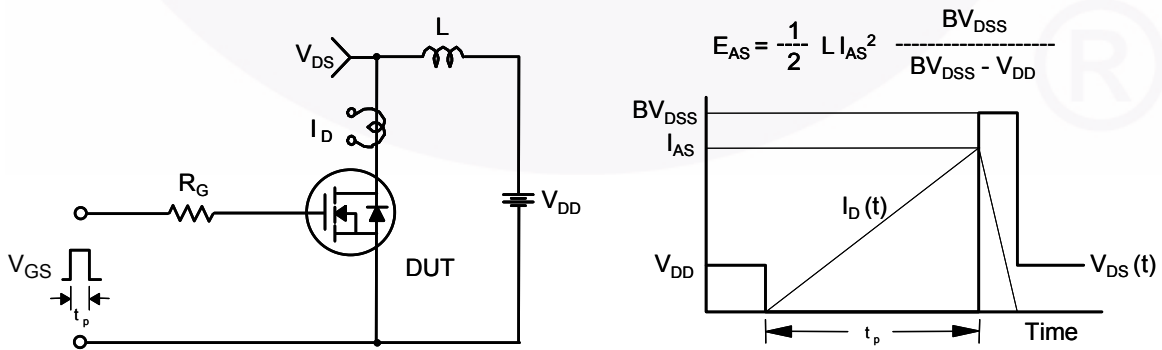
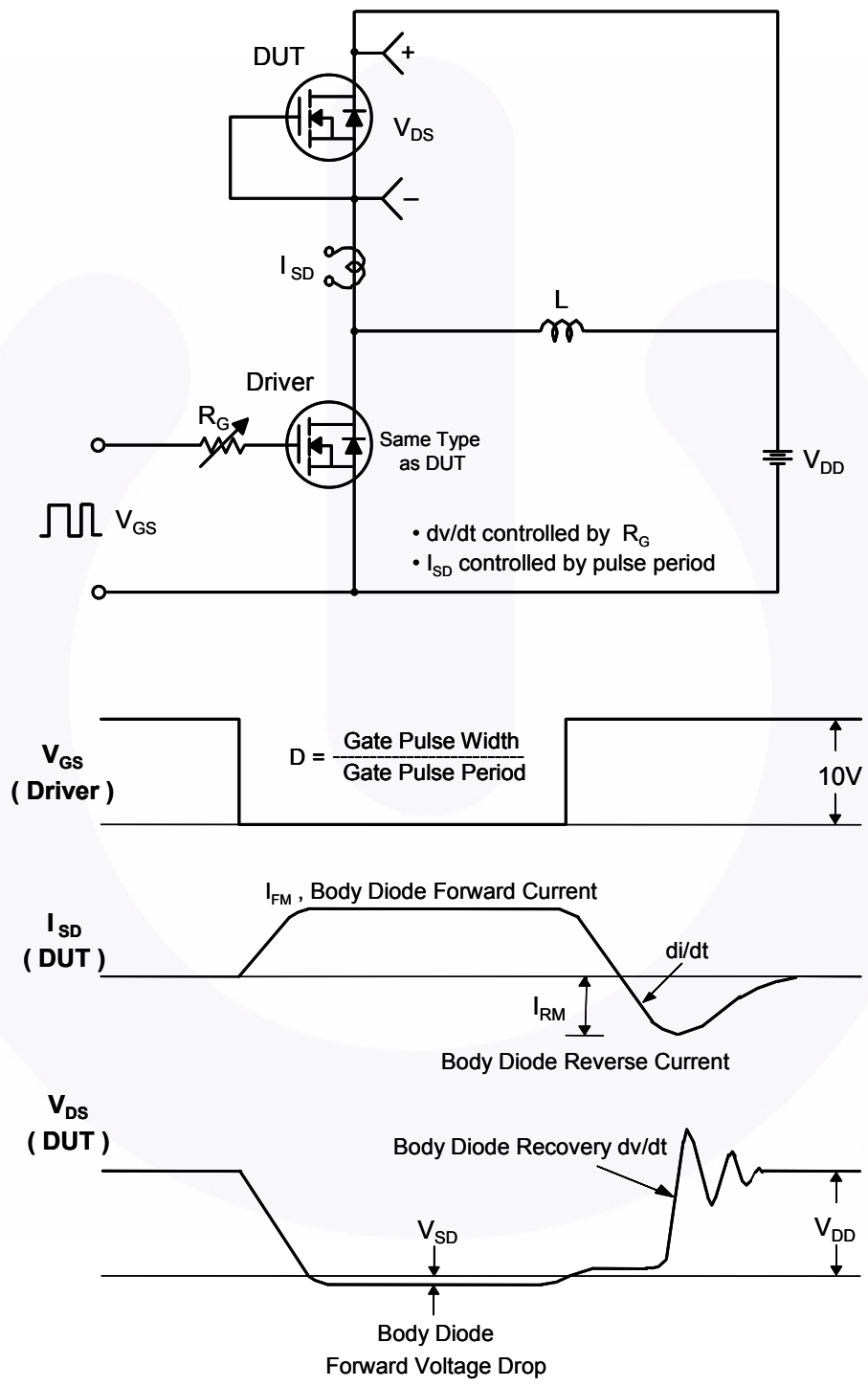
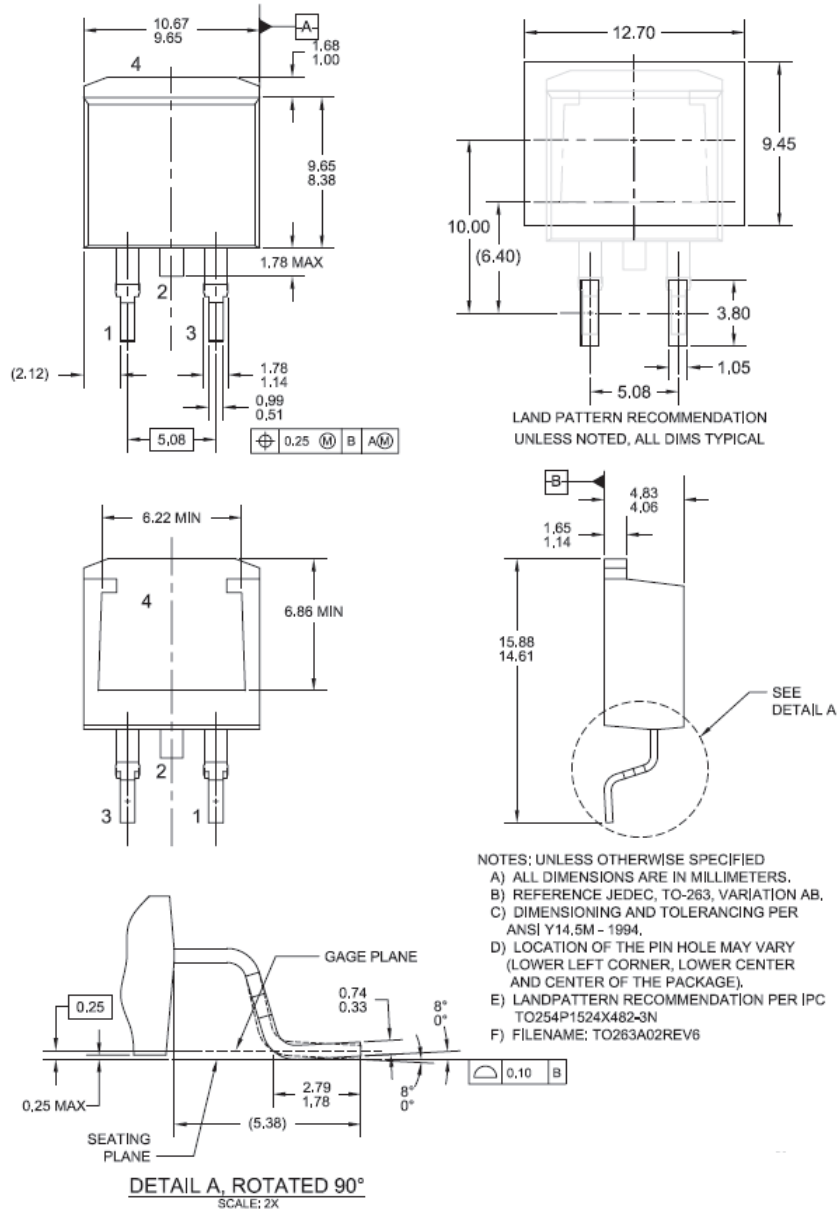


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



**Mechanical Dimensions**

**TO-263 2L (D<sup>2</sup>PAK)**



**Figure 16. 2LD,TO263, Surface Mount**

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Dimension in Millimeters





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