SN74AVC2T245 Dual-Bit Dual-Supply Bus Transceiver with Configurable Level-Shifting / Voltage Translation and Tri-State Outputs

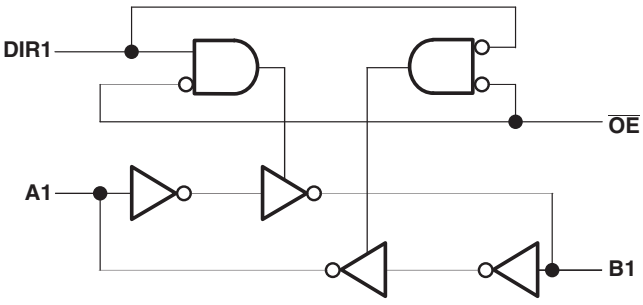
1 Features

- Each Channel Has Independent Direction Control
- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2 V to 3.6 V Power-Supply Range
- I/Os Are 4.6 V Tolerant
- I_{off} Supports Partial-Power-Down Mode Operation
- V_{CC} Isolation Feature - If Either V_{CC} Input is at GND, Both Ports are in High-Impedance State
- Typical Data Rates
  - 500 Mbps (1.8 V to 3.3 V Level-Shifting)
  - 320 Mbps (<1.8 V to 3.3 V Level-Shifting)
  - 320 Mbps (Translate to 2.5 V or 1.8 V)
  - 280 Mbps (Translate to 1.5 V)
  - 240 Mbps (Translate to 1.2 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 5000 V Human-Body Model (A114-A)
  - 200 V Machine Model (A115-A)
  - 1500 V Charged-Device Model (C101)

2 Applications

- Personal Electronics
- Industrial
- Enterprise
- Telecom

Logic Diagram (Positive Logic)



(1) Shown for a single channel

3 Description

This dual-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V voltage nodes.

The SN74AVC2T245 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode . The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

The SN74AVC2T245 control pins (DIR1, DIR2, and $\overline{OE}$) are supplied by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ must be connected to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AVC2T245	UQFN (10)	1.80 mm × 1.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

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4 Revision History

Changes from Revision C (July 2015) to Revision D — **Page**

- Made changes to *Pin Configuration and Functions* ... 1

Changes from Revision B (June 2015) to Revision C — **Page**

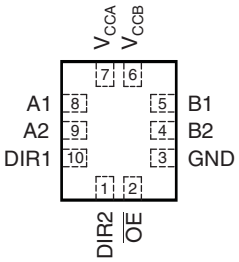
- The *Ordering Information* table (formally on page 1) contained a Top-Side Marking of TQ_. The table has been replaced with the Package Option Addendum in *Mechanical, Packaging, and Orderable Information*. VC_ was added to the device marking 17

Changes from Revision A (May 2012) to Revision B — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed the Ordering Information table. ... 1

5 Pin Configuration and Functions

RSW PACKAGE
10-PIN UQFN
TOP VIEW



Pin Functions

PIN		DESCRIPTION
NAME	NO. (UQFN)	
V_{CCA}	7	Supply Voltage A
V_{CCB}	6	Supply Voltage B
GND	3	Ground
A1	8	Output or input depending on state of DIR. Output level depends on V_{CCA}.
A2	9	Output or input depending on state of DIR. Output level depends on V_{CCA}.
B1	5	Output or input depending on state of DIR. Output level depends on V_{CCB}.
B2	4	Output or input depending on state of DIR. Output level depends on V_{CCB}.
DIR1,DIR2	10,1	Direction Pin, Connect to GND or to V_{CCA}
$\overline{OE}$	2	Tri-state output-mode enables. Pull OE high to place all outputs in 3-state mode. Referenced to V_{CCA}

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage		–0.5	4.6	V
V_I	Input voltage(2)	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_J	Junction Temperature		-40	150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	5000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1) (2) (3)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs(1)	1.2 V to 1.95 V		V_{CCI} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs(1)	1.2 V to 1.95 V			V_{CCI} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})(2)	1.2 V to 1.95 V		V_{CCA} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Recommended Operating Conditions[1] [2] [3] (continued)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})[2]	1.2 V to 1.95 V			V_{CCA} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.1 V to 1.2 V		–3	mA
				1.4 V to 1.6 V		–6	
				1.65 V to 1.95 V		–8	
				2.3 V to 2.7 V		–9	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.1 V to 1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		SN74AVC2T245 RSW (UQFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	18.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = –100 μA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V				V_{CCO} – 0.2		V
		I_{OH} = –3 mA		1.2 V	1.2 V		0.95				
		I_{OH} = –6 mA		1.4 V	1.4 V				1.05		
		I_{OH} = –8 mA		1.65 V	1.65 V				1.2		
		I_{OH} = –9 mA		2.3 V	2.3 V				1.75		
		I_{OH} = –12 mA		3 V	3 V				2.3		
V_{OL}		I_{OL} = 100 μA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V					0.2	V
		I_{OL} = 3 mA		1.2 V	1.2 V		0.25				
		I_{OL} = 6 mA		1.4 V	1.4 V					0.35	
		I_{OL} = 8 mA		1.65 V	1.65 V					0.45	
		I_{OL} = 9 mA		2.3 V	2.3 V					0.55	
		I_{OL} = 12 mA		3 V	3 V					0.7	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V		±0.025	±0.25		±1	μA
I_{off}	A or B port	V_I or V_O = 0 to 3.6 V		0 V	0 V to 3.6 V		±0.1	±1		±5	μA
				0 V to 3.6 V	0 V		±0.1	±1		±5	
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V		±0.5	±2.5		±5	μA
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					8	μA
				0 V	0 V to 3.6 V					–2	
				0 V to 3.6 V	0 V					8	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					8	μA
				0 V	0 V to 3.6 V					8	
				0 V to 3.6 V	0 V					–2	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					16	μA
C_i	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V		3.5			4.5	pF
C_{io}	A or B port	V_O = 3.3 V or GND		3.3 V	3.3 V		6			7	pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.

6.6 Switching Characteristics: V_{CCA} = 1.2 V

over recommended operating free-air temperature range, V_{CCA} = 1.2 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V	V_{CCB} = 1.8 V ± 0.15 V	V_{CCB} = 2.5 V ± 0.2 V	V_{CCB} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t_{PLH}	A	B	2.5	2.1	1.9	1.9	1.9	ns
t_{PHL}			2.5	2.1	1.9	1.9	1.9	
t_{PLH}	B	A	2.5	2.2	2	1.8	1.7	ns
t_{PHL}			2.5	2.2	2	1.8	1.7	
t_{PZH}	$\overline{OE}$	A	3.8	3.1	2.7	2.6	3	ns
t_{PZL}			3.8	3.1	2.7	2.6	3	
t_{PZH}	$\overline{OE}$	B	3.7	3.7	3.7	3.7	3.7	ns
t_{PZL}			3.7	3.7	3.7	3.7	3.7	
t_{PHZ}	$\overline{OE}$	A	4.4	3.6	3.5	3.3	4.1	ns
t_{PLZ}			4.4	3.6	3.5	3.3	4.1	
t_{PHZ}	$\overline{OE}$	B	4.2	4.2	4.3	4.1	4.2	ns
t_{PLZ}			4.2	4.2	4.3	4.1	4.2	

6.7 Switching Characteristics: V_{CCA} = 1.5 V ± 0.1 V

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.2	0.3	4.4	0.2	3.9	0.1	3.6	0.1	3.9	ns
t_{PHL}			2.2	0.3	4.4	0.2	3.9	0.1	3.6	0.1	3.9	
t_{PLH}	B	A	2	0.6	5.1	0.4	4.9	0.2	4.6	0.1	4.5	ns
t_{PHL}			2	0.6	5.1	0.4	4.9	0.2	4.6	0.1	4.5	
t_{PZH}	$\overline{OE}$	A	3.4	1.1	7.1	0.9	6.2	0.7	5.5	0.1	6.4	ns
t_{PZL}			3.4	1.1	7.1	0.9	6.2	0.7	5.5	0.1	6.4	
t_{PZH}	$\overline{OE}$	B	2.5	1.1	8.2	1.1	8.2	1.1	8.2	1.1	8.2	ns
t_{PZL}			2.5	1.1	8.2	1.1	8.2	1.1	8.2	1.1	8.2	
t_{PHZ}	$\overline{OE}$	A	4.1	1.2	7.1	0.8	6.7	0.4	5.6	1	74	ns
t_{PLZ}			4.1	1.2	7.1	0.8	6.7	0.4	5.6	1	7.4	
t_{PHZ}	$\overline{OE}$	B	3.3	0.3	7.4	0.2	5.7	0.3	5.6	0.3	5.6	ns
t_{PLZ}			3.3	0.3	7.4	0.2	5.7	0.3	5.6	0.3	5.6	

6.8 Switching Characteristics: V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	0.1	4.1	0.1	3.6	0.1	3.1	0.1	3.3	ns
t_{PHL}			2	0.1	4.1	0.1	3.6	0.1	3.1	0.1	3.3	
t_{PLH}	B	A	1.9	0.4	4.3	0.1	4.1	0.1	3.8	0.1	3.7	ns
t_{PHL}			1.9	0.4	4.3	0.1	4.1	0.1	3.8	0.1	3.7	
t_{PZH}	$\overline{OE}$	A	3.2	0.8	6.7	0.4	5.8	0.4	4.8	0.3	4.6	ns
t_{PZL}			3.2	0.8	6.7	0.4	5.8	0.4	4.8	0.3	4.6	
t_{PZH}	$\overline{OE}$	B	1.9	0.2	6.7	0.2	6.6	0.2	6.7	0.2	6.7	ns
t_{PZL}			1.9	0.2	6.7	0.2	6.6	0.2	6.7	0.2	6.7	
t_{PHZ}	$\overline{OE}$	A	3.8	0.7	6.2	0.3	6.5	0.1	5.2	0.8	6.5	ns
t_{PLZ}			3.8	0.7	6.2	0.3	6.5	0.1	5.2	0.8	6.5	
t_{PHZ}	$\overline{OE}$	B	3.4	0.1	6.8	0.1	6.8	0.1	6.7	0.1	6.7	ns
t_{PLZ}			3.4	0.1	6.8	0.1	6.8	0.1	6.7	0.1	6.7	

6.9 Switching Characteristics: V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.9	0.1	3.8	0.1	3.2	0.1	2.7	0.1	2.6	ns
t_{PHL}			1.9	0.1	3.8	0.1	3.2	0.1	2.7	0.1	2.6	
t_{PLH}	B	A	1.8	0.5	3.4	0.2	3.1	0.1	2.8	0.1	2.6	ns
t_{PHL}			1.8	0.5	3.4	0.2	3.1	0.1	2.8	0.1	2.6	
t_{PZH}	$\overline{OE}$	A	3.1	0.7	6.2	0.5	5.2	0.3	4.1	0.3	3.6	ns
t_{PZL}			3.1	0.7	6.2	0.5	5.2	0.3	4.1	0.3	3.6	
t_{PZH}	$\overline{OE}$	B	1.4	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns
t_{PZL}			1.4	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	
t_{PHZ}	$\overline{OE}$	A	3.6	0.2	5.2	0.1	5.4	0.1	4.5	0.7	6	ns
t_{PLZ}			3.6	0.2	5.2	0.1	5.4	0.1	4.5	0.7	6	
t_{PHZ}	$\overline{OE}$	B	2.1	0.1	4.7	0.1	4.6	0.1	4.7	0.1	4.7	ns
t_{PLZ}			2.1	0.1	4.7	0.1	4.6	0.1	4.7	0.1	4.7	

6.10 Switching Characteristics: V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.8	0.1	3.6	0.1	3	0.1	2.6	0.1	2.4	ns
t_{PHL}			1.8	0.1	3.6	0.1	3	0.1	2.6	0.1	2.4	
t_{PLH}	B	A	1.9	0.5	3.4	0.2	2.9	0.1	2.5	0.1	2.3	ns
t_{PHL}			1.9	0.5	3.4	0.2	2.9	0.1	2.5	0.1	2.3	
t_{PZH}	$\overline{OE}$	A	3.1	0.9	5.9	0.5	5	0.3	3.8	0.3	3.3	ns
t_{PZL}			3.1	0.9	5.9	0.5	5	0.3	3.8	0.3	3.3	
t_{PZH}	$\overline{OE}$	B	1.2	0.4	3.6	0.4	3.6	0.4	3.6	0.4	3.6	ns
t_{PZL}			1.2	0.4	3.6	0.4	3.6	0.4	3.6	0.4	3.6	
t_{PHZ}	$\overline{OE}$	A	3.4	0.1	4.6	0.1	4.7	0.3	4.8	0.7	4.5	ns
t_{PLZ}			3.4	0.1	4.6	0.1	4.7	0.3	4.8	0.7	4.5	
t_{PHZ}	$\overline{OE}$	B	2.9	0.1	5.4	0.1	5.3	0.1	5.3	0.1	5.3	ns
t_{PLZ}			2.9	0.1	5.4	0.1	5.3	0.1	5.3	0.1	5.3	

6.11 Operating Characteristics

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.2 V	V_{CCA} = V_{CCB} = 1.5 V	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C_{pdA} (1)	A to B	Outputs enabled	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns	3	3	3	3	4	pF
		Outputs disabled		1	1	1	2	2	
	B to A	Outputs enabled		12	13	13	15	15	
		Outputs disabled		1	2	2	2	2	
C_{pdB} (1)	A to B	Outputs enabled	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns	12	13	13	14	16	pF
		Outputs disabled		1	2	2	2	2	
	B to A	Outputs enabled		3	3	3	4	4	
		Outputs disabled		1	1	1	2	2	

(1) Power dissipation capacitance per transceiver. Refer to the TI application report, CMOS Power Consumption and Cpd Calculation, SCAA035

6.12 Typical Characteristics

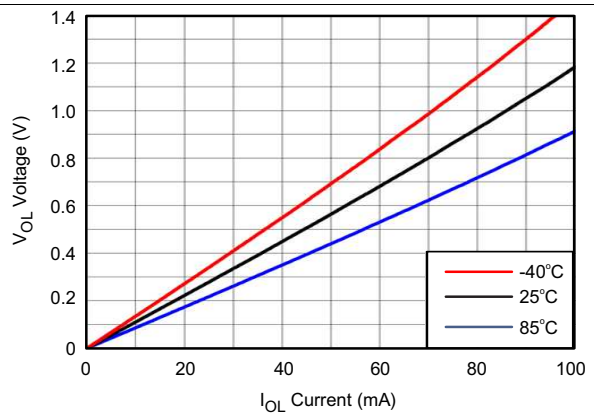


Figure 1. V_{OL} Voltage vs I_{OL} Current

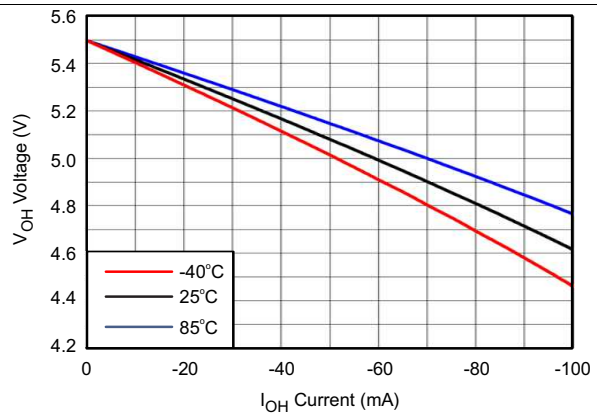
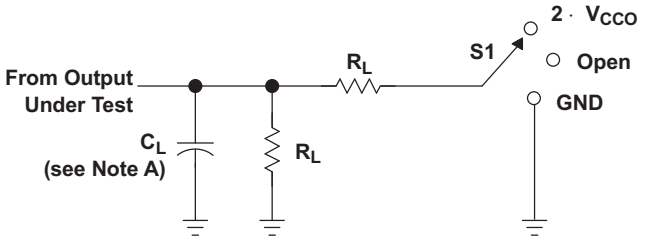


Figure 2. V_{OH} Voltage vs I_{OH} Current

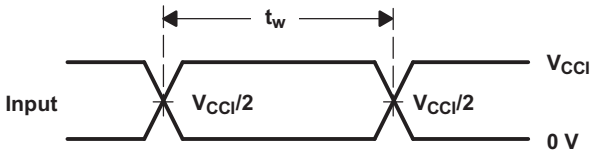
7 Parameter Measurement Information



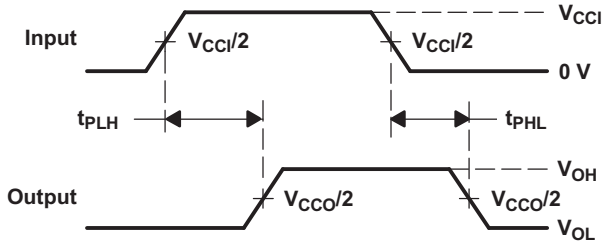
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 · V_{CCO}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

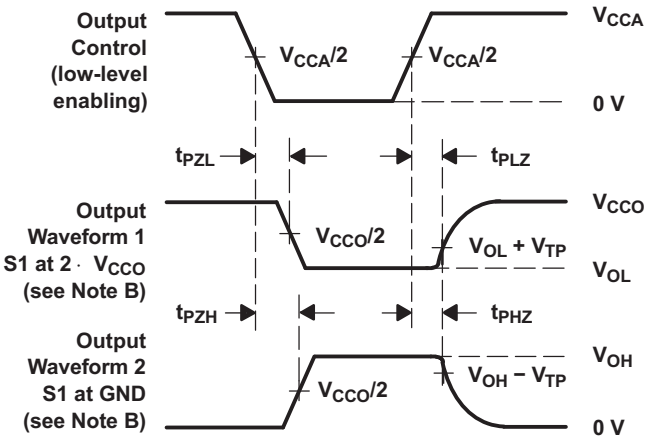
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.
F. V_{CCI} is the V_{CC} associated with the input port.
G. V_{CCO} is the V_{CC} associated with the output port.

Figure 3. Load and Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74AVC2T245 is a dual-bit, dual-supply noninverting bidirectional voltage level translation. Pins A and control pins (DIR and $\overline{OE}$) are supported by V_{CCA} and pins B are supported by V_{CCB}. The A port can accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.2 V to 3.6 V. A high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both A and B are in the high-impedance state.

This device is fully specified for partial-power-down applications using off output current (I_{off}).

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are put in a high-impedance state.

8.2 Functional Block Diagram

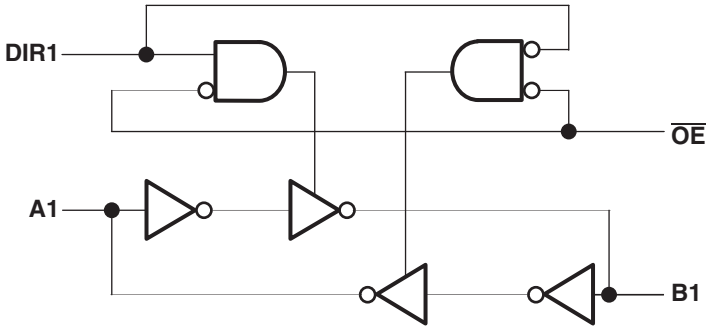


Figure 4. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2 V to 3.6 V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage from 1.2 V to 3.6 V making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.8 V, 2.5 V, and 3.3 V).

8.3.2 Partial-Power-Down Mode Operation

This device is fully specified for partial-power-down applications using off output current (I_{off}). The I_{off} circuitry will prevent backflow current by disabling I/O output circuits when device is in partial power-down mode.

8.3.3 V_{CC} Isolation

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} are at GND, both ports will be in a high-impedance state (I_{OZ}). This prevents false logic levels from being presented to either bus.

8.4 Device Functional Modes

The SN74AVC2T245 is a voltage level translator that can operate from1.2 V to 3.6 V (V_{CCA}) and 1.2 V to 3.6 V (V_{CCB}). The signal translation requires direction control and output enable control. The table below enlists the operation of the part for the respective states of the control inputs.

Table 1. Function Table(1) (Each Transceiver)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR1	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AVC2T45 is used to shift IO voltage levels from one voltage domain to another. Bus A and bus B have independent power supplies, and a direction pin is used to control the direction of data flow. Unused data ports must not be floating; tie the unused port input and output to ground directly.

9.1.1 Enable Times

Calculate the enable times for the SN74AVC16T45 using the following formulas:

t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A) (1)

t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A) (2)

t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B) (3)

t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B) (4)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVC2T245 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

9.2 Typical Application

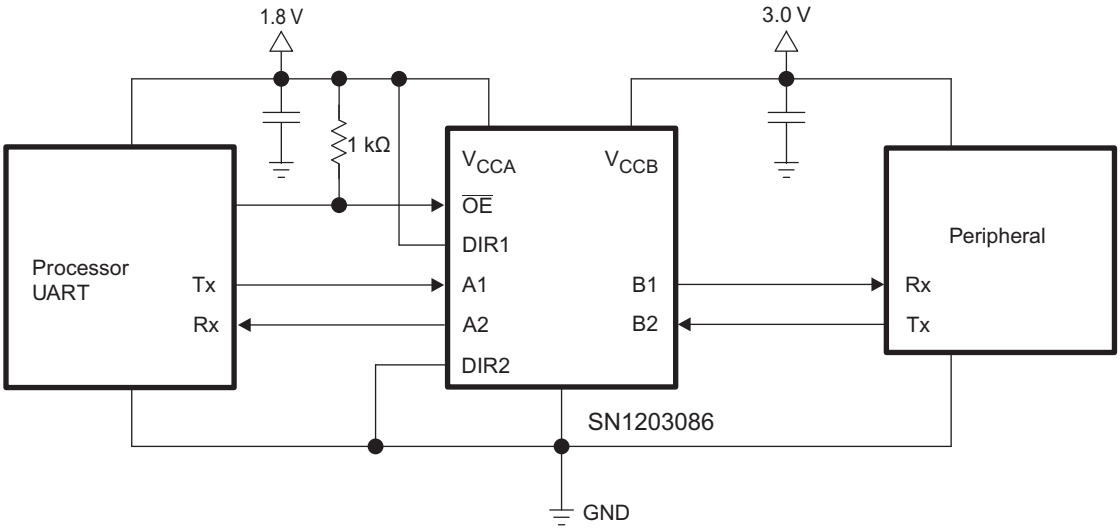


Figure 5. Typical Application of the SN74AVC2T245

9.2.1 Design Requirements

This device uses drivers which are enabled depending on the state of the DIR pin. The designer must know the intended flow of data and take care not to violate any of the high or low logic levels. Unused data inputs must not be floating, as this can cause excessive internal leakage on the input CMOS structure. Tie any unused input and output ports directly to ground.

For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.2 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

9.2.2.1 Input Voltage Ranges

Use the supply voltage of the device that is driving the SN74AVC2T245 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.

9.2.2.2 Output Voltage Range

Use the supply voltage of the device that the SN74AVC2T245 device is driving to determine the output voltage range.

9.2.3 Application Curves

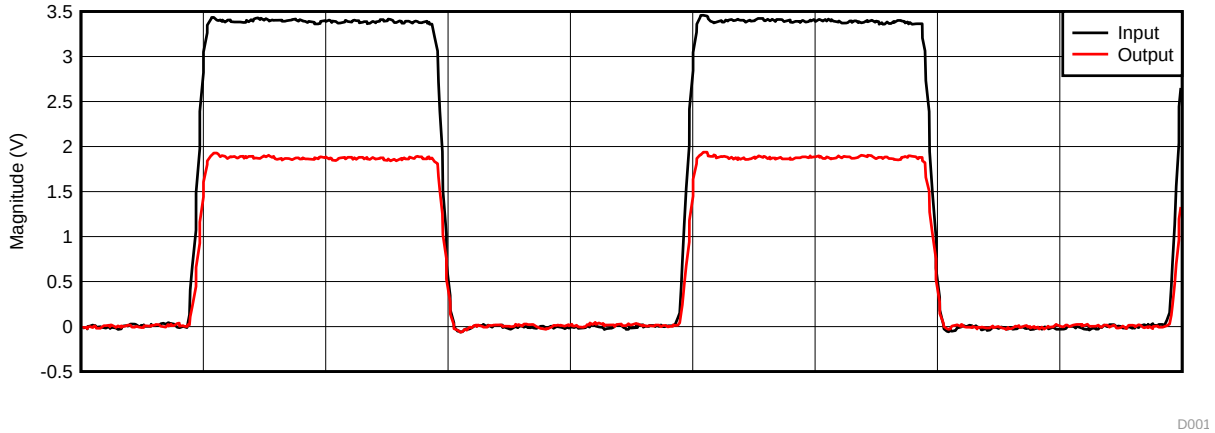


Figure 6. 3.3 V to 1.8 V Level-Shifting With 1-MHz Square Wave

10 Power Supply Recommendations

The SN74AVC2T245 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V and V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage bidirectional translation between any of the 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5 V voltage nodes.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit-board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

11.2 Layout Example

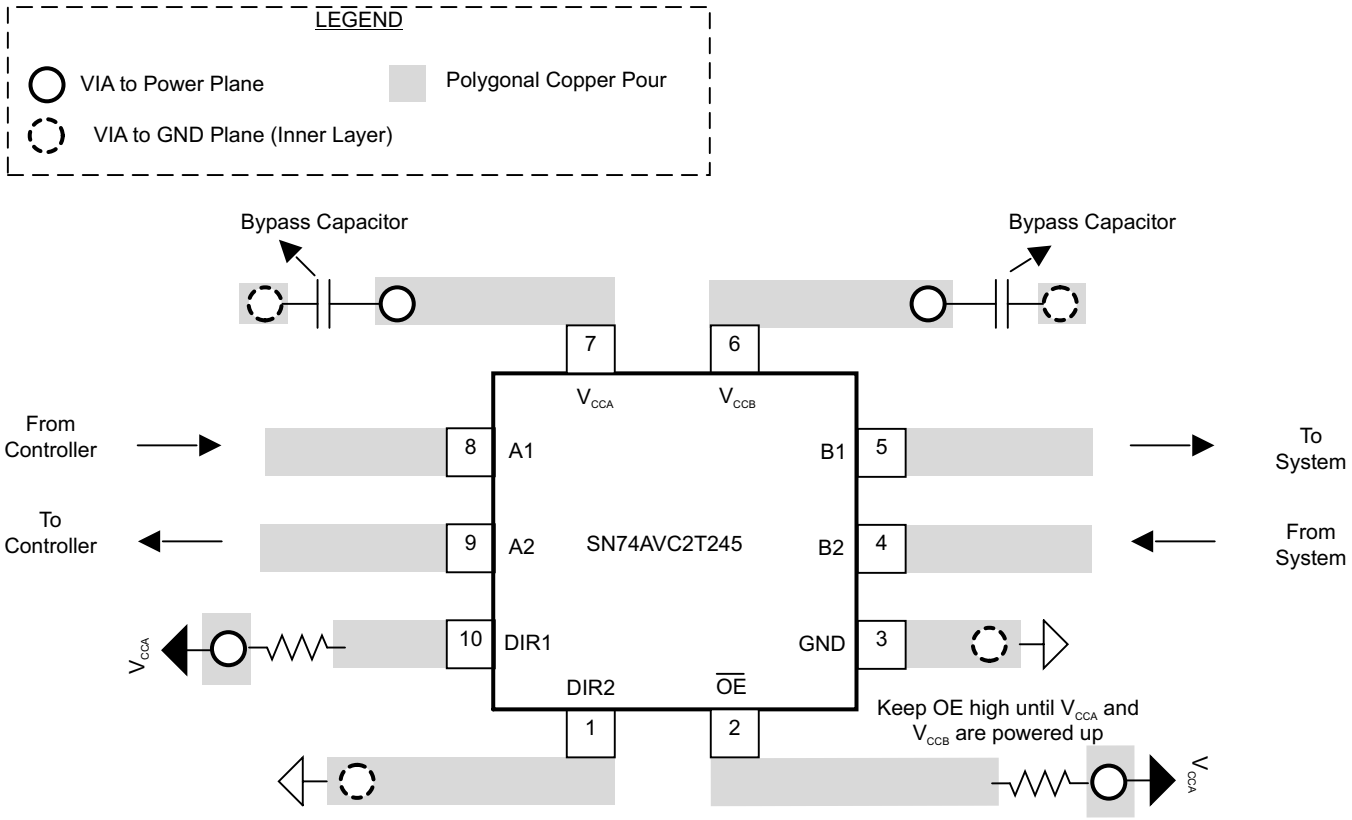


Figure 7. Recommended Layout Example

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AVC2T245RSWR	ACTIVE	UQFN	RSW	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(TQ7, TQO, TQR, TQV) (TQH, TQJ, TQY) (VCH, VCO) (VCJ, VCR)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

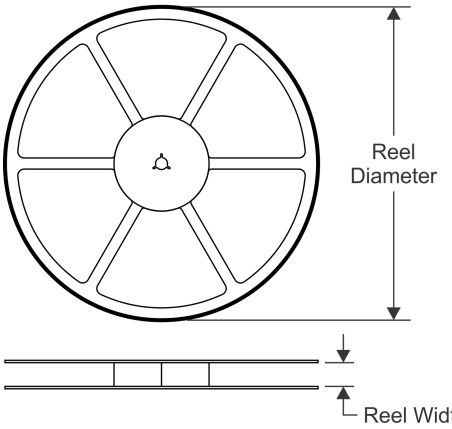
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

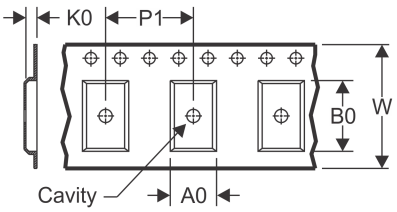
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

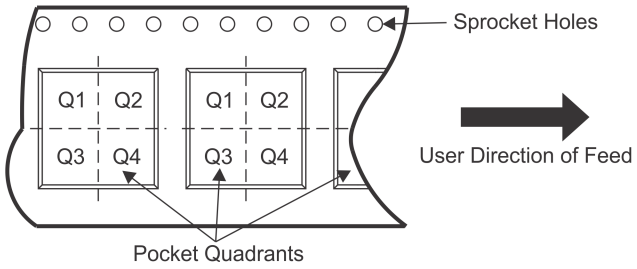


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

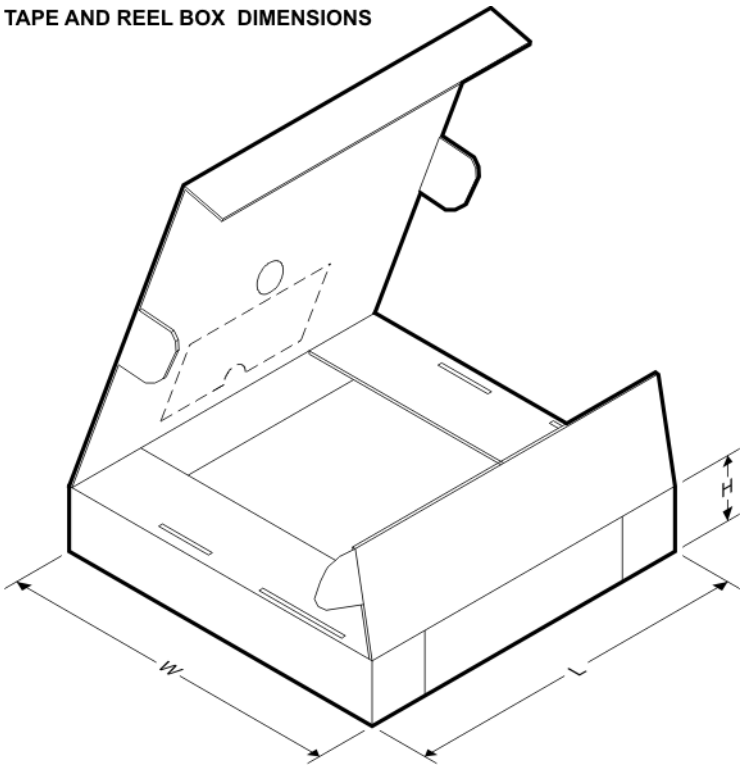
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC2T245RSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
SN74AVC2T245RSWR	UQFN	RSW	10	3000	180.0	8.4	1.59	2.09	0.72	4.0	8.0	Q1
SN74AVC2T245RSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
SN74AVC2T245RSWR	UQFN	RSW	10	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q1

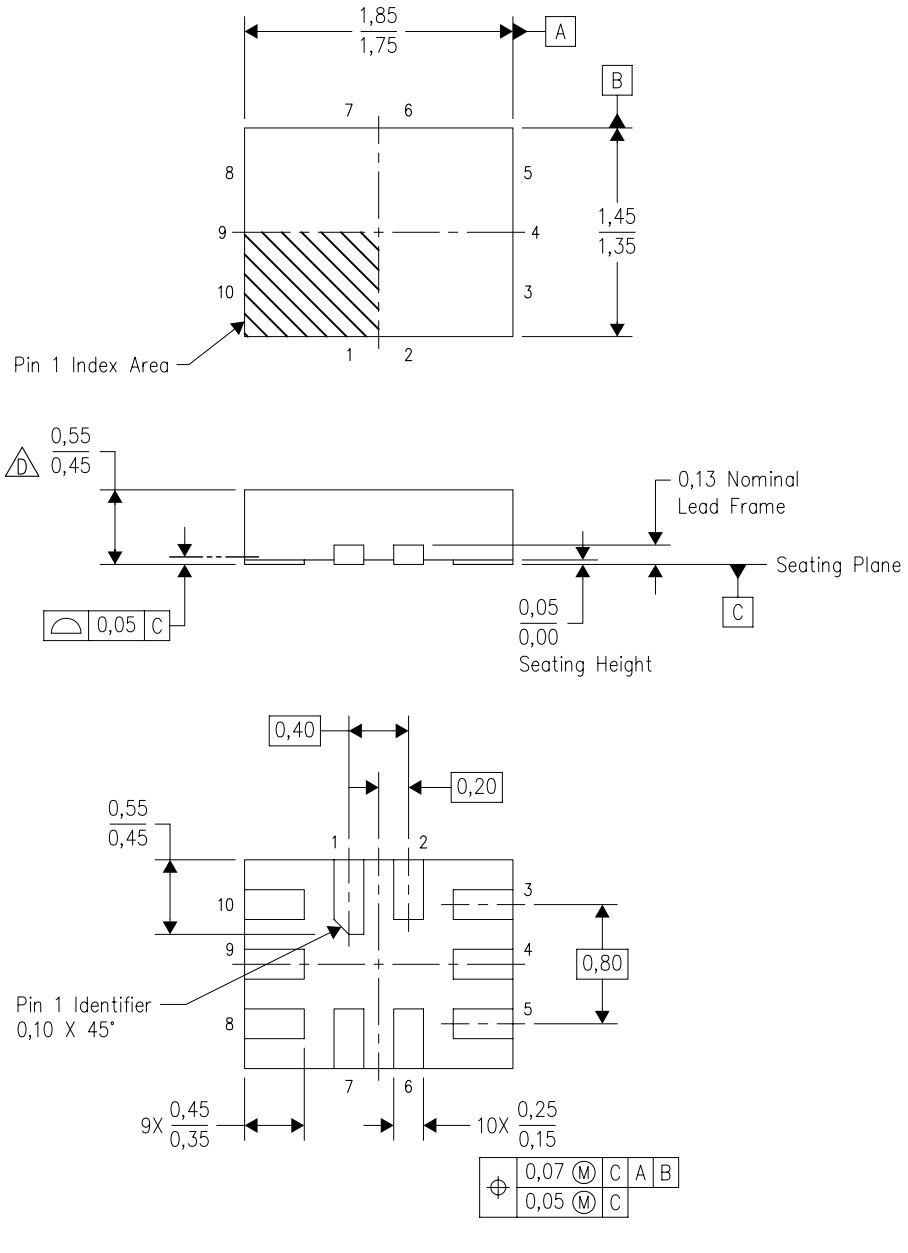
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC2T245RSWR	UQFN	RSW	10	3000	189.0	185.0	36.0
SN74AVC2T245RSWR	UQFN	RSW	10	3000	202.0	201.0	28.0
SN74AVC2T245RSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
SN74AVC2T245RSWR	UQFN	RSW	10	3000	184.0	184.0	19.0

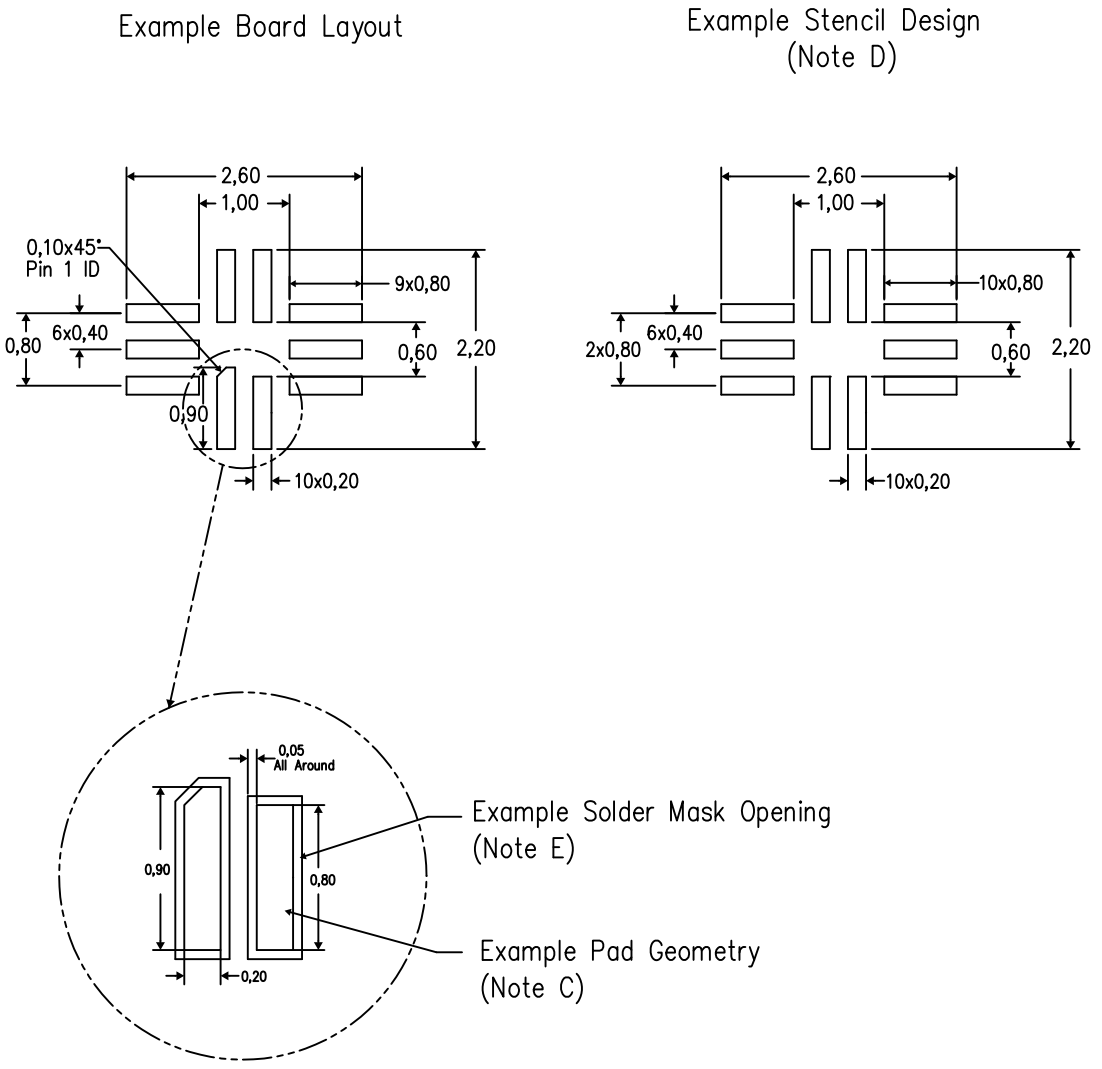
RSW (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



4208097/C 07/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–lead) package configuration.
D. This package complies to JEDEC MO–288 variation UDEE, except minimum package height.

RSW (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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