

CD40160B, CD40161B, CD40162B, CD40163B Types

CMOS Synchronous Programmable 4-Bit Counters

High-Voltage Types (20-Volt Rating)

CD40160B – Decade with Asynchronous Clear

CD40161B – Binary with Asynchronous Clear

CD40162B – Decade with Synchronous Clear

CD40163B – Binary with Synchronous Clear

■ CD40160B, CD40161B, CD40162B, and CD40163B are 4-bit synchronous programmable counters. The CLEAR function of the CD40162B and CD40163B is synchronous and a low level at the CLEAR input sets all four outputs low on the next positive CLOCK edge. The CLEAR function of the CD40160B and CD40161B is asynchronous and a low level at the CLEAR input sets all four outputs low regardless of the state of the CLOCK, LOAD, or ENABLE inputs. A low level at the LOAD input disables the counter and causes the output to agree with the setup data after the next CLOCK pulse regardless of the conditions of the ENABLE inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output (C_{OUT}). Counting is enabled when both PE and TE inputs are high. The TE input is fed forward to enable C_{OUT}. This enabled output produces a positive output pulse with a

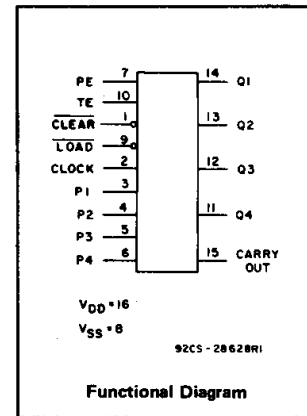
Features:

- Internal look-ahead for fast counting
- Carry output for cascading
- Synchronously programmable
- Clear asynchronous input (CD40160B, CD40161B)
- Clear synchronous input (CD40162B, CD40163B)
- Synchronous load control input
- Low-power TTL compatibility
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages. Logic transitions at the PE or TE inputs may occur when the clock is either high or low.

The CD40160B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix). The CD40161B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

The CD40160B through CD40163B types are functionally equivalent to and pin-compatible with the TTL counter series 74LS160 through 74LS163 respectively.



Applications:

- Programmable binary and decade counting
- Counter control/timers
- Frequency dividing

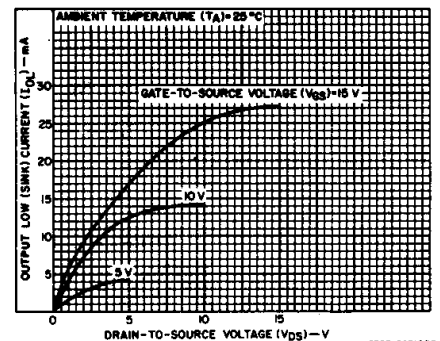


Fig. 1 – Typical output low (sink) current characteristics.

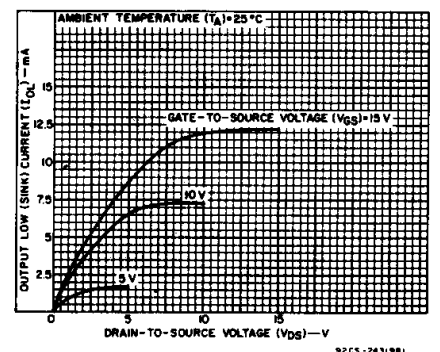


Fig. 2 – Minimum output low (sink) current characteristics.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT ±10mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -55°C to +100°C 500mW

For T_A = +100°C to +125°C Derate Linearly at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max +285°C

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD40160B, CD40161B, CD40162B, CD40163B Types

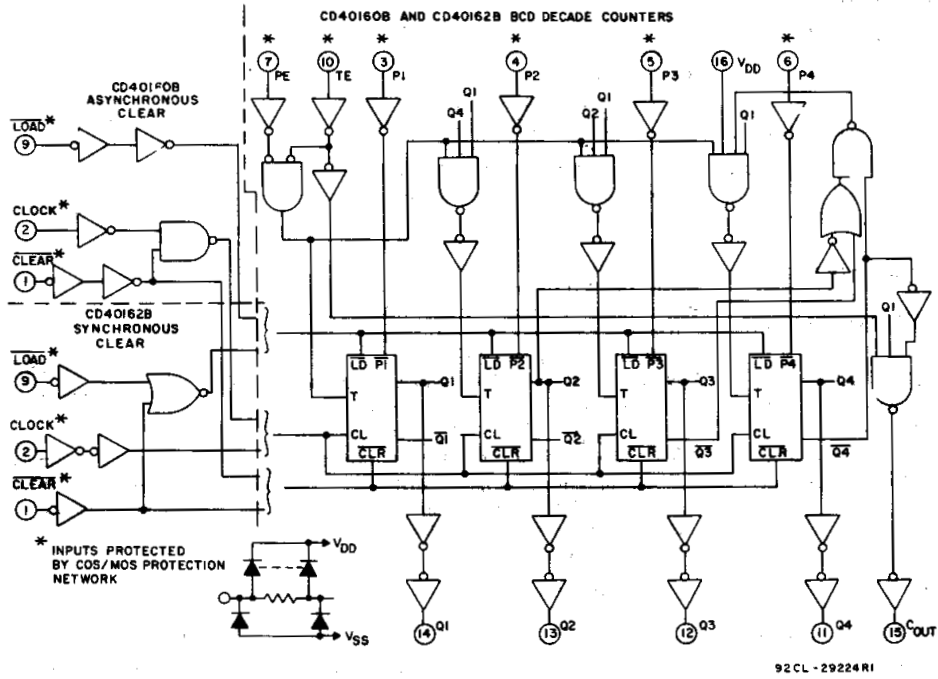


Fig. 3— Logic diagrams for CD40160B and CD40162B BCD decade counters.

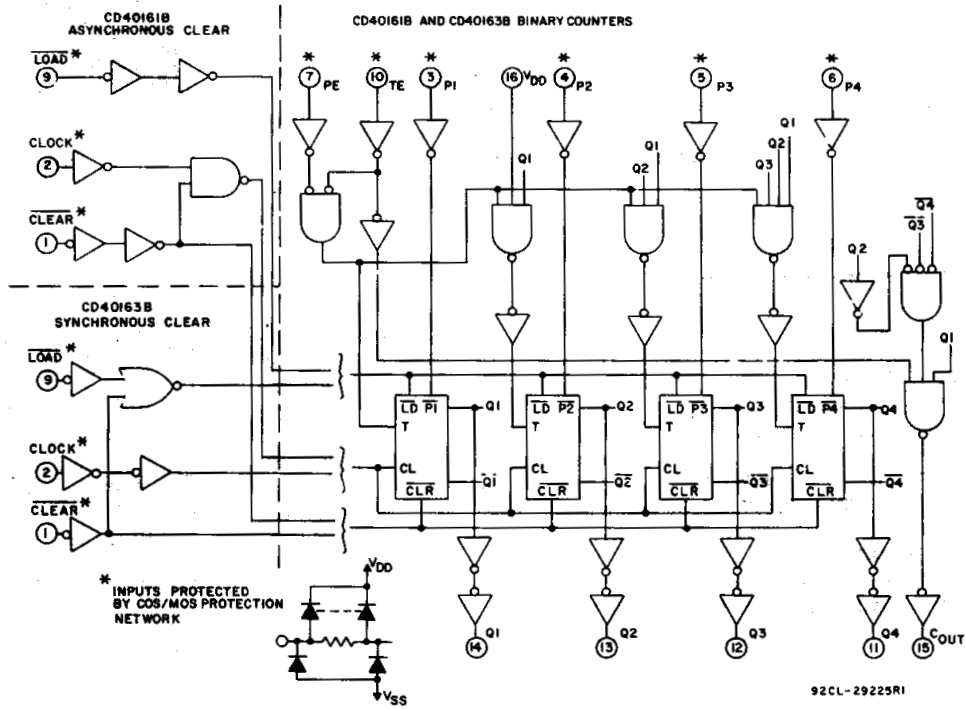


Fig. 4— Logic diagrams for CD40161B and CD40163B binary counters.

CD40160B, CD40161B, CD40162B, CD40163B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply Voltage Range (Full T_A = Full Package-Temperature Range)	—	3	18	V
Setup Time: t_{SU} Data to Clock	5	240	—	ns
	10	90	—	
	15	60	—	
Load to Clock	5	240	—	ns
	10	90	—	
	15	60	—	
PE or TE to Clock	5	340	—	ns
	10	140	—	
	15	100	—	
Clear to Clock (CD40162B, CD40163B)	5	340	—	ns
	10	140	—	
	15	100	—	
All Hold Times, t_H	5	0	—	ns
	10	0	—	
	15	0	—	
Clear Removal Time, t_{rem} (CD40160B, CD40161B)	5	200	—	ns
	10	100	—	
	15	70	—	
Clear Pulse Width, t_{WL} (CD40160B, CD40161B)	5	170	—	ns
	10	70	—	
	15	50	—	
Clock Input Frequency, f_{CL}	5	—	2	MHz
	10	—	5.5	
	15	—	8	
Clock Pulse Width, t_W	5	170	—	ns
	10	70	—	
	15	50	—	
Clock Rise or Fall Time, t_{rCL} or t_{fCL}	5	—	200	μs
	10	—	70	
	15	—	15	

TRUTH TABLE

CLOCK	$\overline{\text{CLR}}$	$\overline{\text{LOAD}}$	PE	TE	OPERATION
	1	0	X	X	PRESET
	1	1	0	X	NC
	1	1	X	0	NC
	1	1	1	1	COUNT
X	0	X	X	X	RESET (CD40160B, CD40161B)
	0	X	X	X	RESET (CD40162B, CD40163B)
	1	X	X	X	NC (CD40162B, CD40163B)

1 = HIGH LEVEL 0 = LOW LEVEL X = DON'T CARE NC = NO CHANGE

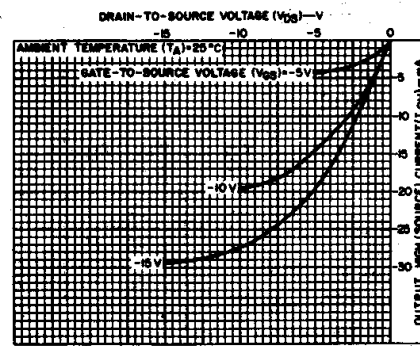


Fig. 5— Typical output high (source) current characteristics.

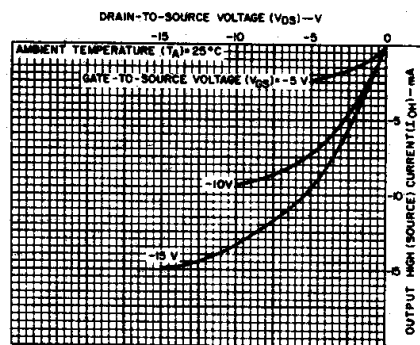


Fig. 6— Minimum output high (source) current characteristics.

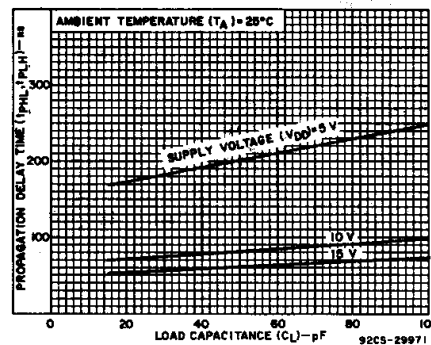


Fig. 7— Typical propagation delay time as a function of load capacitance (CLOCK to Q).

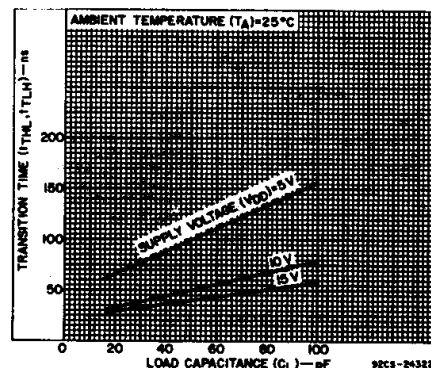


Fig. 8— Typical transition time as a function of load capacitance.

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD40160B, CD40161B, CD40162B, CD40163B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	5	5	150	150	—	0,04	5	μA
	—	0,10	10	10	10	300	300	—	0,04	10	
	—	0,15	15	20	20	600	600	—	0,04	20	
	—	0,20	20	100	100	3000	3000	—	0,08	100	
Output Low (Sink) Current, I _{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	—	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	—	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	—	
Output High (Source) Current, I _{OH} Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	—	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	—	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	—	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0,05				—	0	0,05	V
	—	0,10	10	0,05				—	0	0,05	
	—	0,15	15	0,05				—	0	0,05	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4,95				4,95	5	—	V
	—	0,10	10	9,95				9,95	10	—	
	—	0,15	15	14,95				14,95	15	—	
Input Low Voltage, V _{IL} Max.	0,5,4,5	—	5	1,5				—	—	1,5	V
	1,9	—	10	3				—	—	3	
	1,5,13,5	—	15	4				—	—	4	
Input High Voltage, V _{IH} Min.	0,5,4,5	—	5	3,5				3,5	—	—	V
	1,9	—	10	7				7	—	—	
	1,5,13,5	—	15	11				11	—	—	
Input Current, I _{IN} Max.	—	0,18	18	±0,1	±0,1	±1	±1	—	±10 ⁻⁵	±0,1	μA

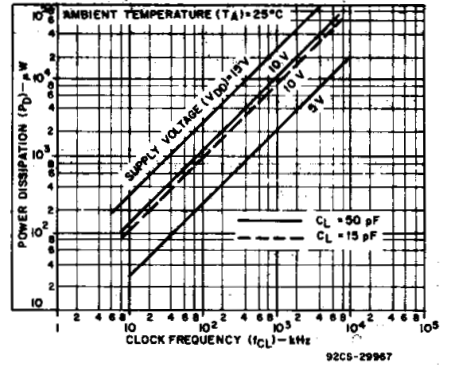


Fig. 9— Typical power dissipation as a function of CLOCK frequency.

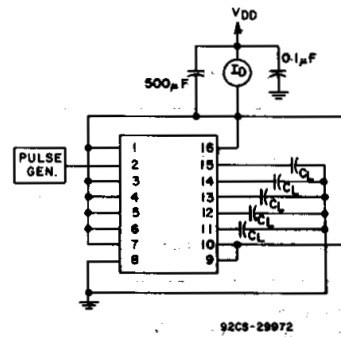


Fig. 10— Dynamic power dissipation test circuit.

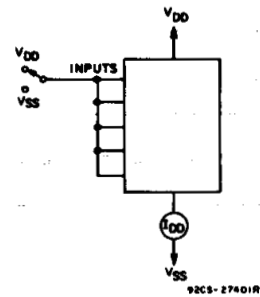


Fig. 11— Quiescent-device-current test circuit.

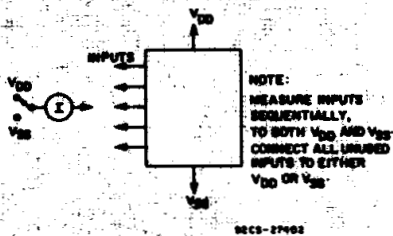


Fig. 12— Input-current test circuit.

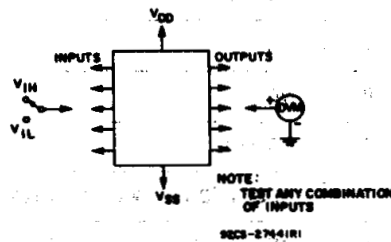


Fig. 13— Input-voltage test circuit.

TERMINAL ASSIGNMENT

CLEAR	1	16	V _{DD}
CLOCK	2	15	CARRY OUT
P1	3	14	Q1
P2	4	13	Q2
P3	5	12	Q3
P4	6	11	Q4
PE	7	10	TE
V _{SS}	8	9	LOAD

92CS-29459

CD40160B, CD40161B, CD40162B, CD40163B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$;
 Input $t_r, t_f = 20 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS ALL TYPES*			UNITS
		Min.	Typ.	Max.	
CLOCK OPERATION					
Propagation Delay Time, t_{PHL}, t_{PLH} Clock to Q	5	—	200	400	ns
	10	—	80	160	
	15	—	60	120	
Clock to C_{OUT}	5	—	225	450	ns
	10	—	95	190	
	15	—	70	140	
TE to C_{OUT}	5	—	125	250	ns
	10	—	55	110	
	15	—	40	80	
Minimum Setup Time, t_{SU} Data to Clock	5	—	120	240	ns
	10	—	45	90	
	15	—	30	60	
Load to Clock	5	—	120	240	ns
	10	—	45	90	
	15	—	30	60	
PE to TE to Clock	5	—	170	340	ns
	10	—	70	140	
	15	—	50	100	
Minimum Hold Time, t_H	5	—	—	0	ns
	10	—	—	0	
	15	—	—	0	
Transition Time, t_{THL}, t_{TLH}	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Minimum Clock Pulse Width, t_W	5	—	85	170	ns
	10	—	35	70	
	15	—	25	50	
Maximum Clock Frequency, f_{CL}	5	2	3	—	MHz
	10	5.5	8.5	—	
	15	8	12	—	
Maximum Clock Rise or Fall Time, † t_{rCL}, t_{fCL}	5	200	—	—	μs
	10	70	—	—	
	15	15	—	—	
CLEAR OPERATION					
Propagation Delay Time, t_{PHL} (CD40160B, CD40161B) Clear to Q	5	—	250	500	ns
	10	—	110	220	
	15	—	80	160	
Minimum Setup Time, t_{SU} (CD40162B, CD40163B) Clear to Clock	5	—	170	340	ns
	10	—	70	140	
	15	—	50	100	
Minimum Hold Time, t_H (CD40162B, CD40163B) Clear to Clock	5	—	—	0	ns
	10	—	—	0	
	15	—	—	0	
Minimum Clear Removal Time, t_{rem} (CD40160B, CD40161B)	5	—	100	200	ns
	10	—	50	100	
	15	—	35	70	
Minimum Clear Pulse Width, t_{WL} (CD40160B, CD40161B)	5	—	85	170	ns
	10	—	35	70	
	15	—	25	50	

* Except as noted.

† If more than one unit is cascaded in the parallel clocked application, t_{rCL} should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the carry output driving stage for the estimated capacitive load.

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD40160B, CD40161B, CD40162B, CD40163B Types

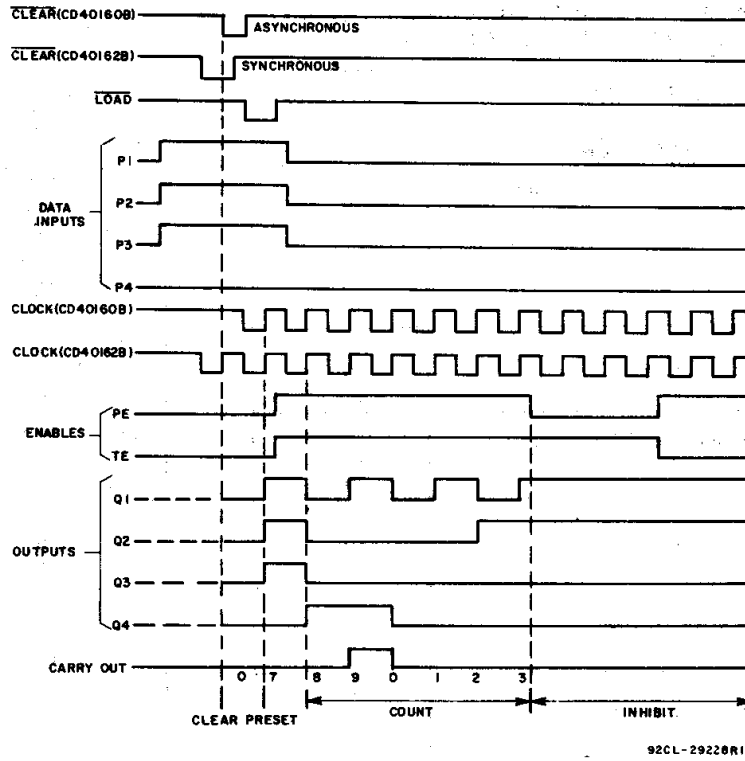


Fig. 14— Timing diagram for CD40160B, CD40162B.

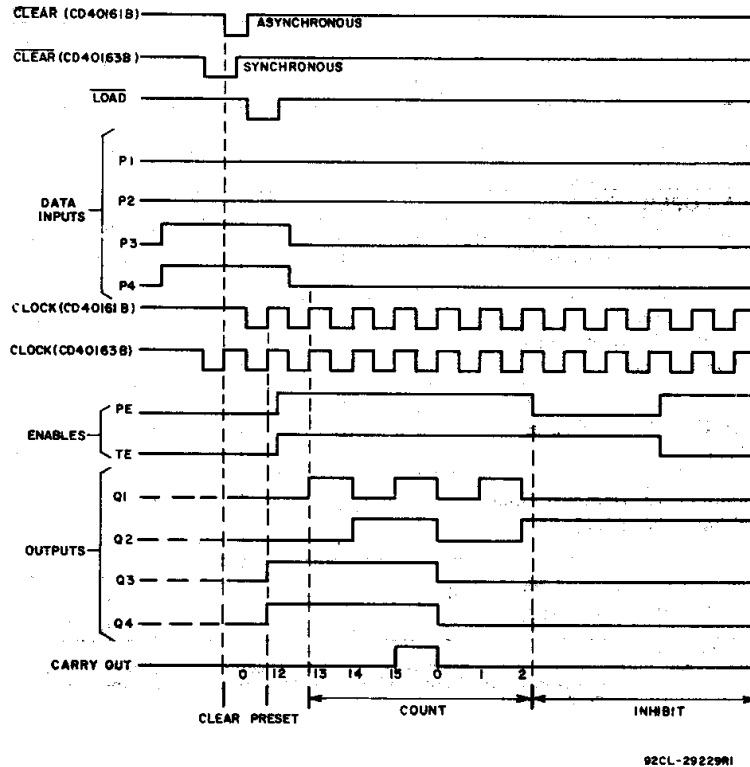


Fig. 15— Timing diagram for CD40161B, CD40163B.

CD40160B, CD40161B, CD40162B, CD40163B Types

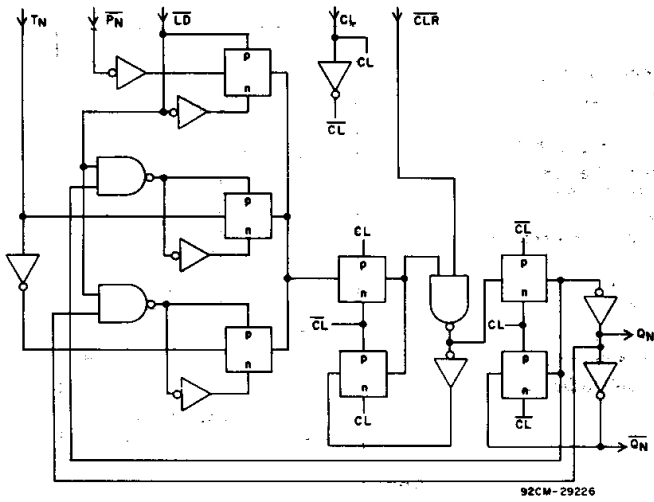


Fig. 16— Detail of flip-flops of CD40160B and CD40161B (asynchronous clear).

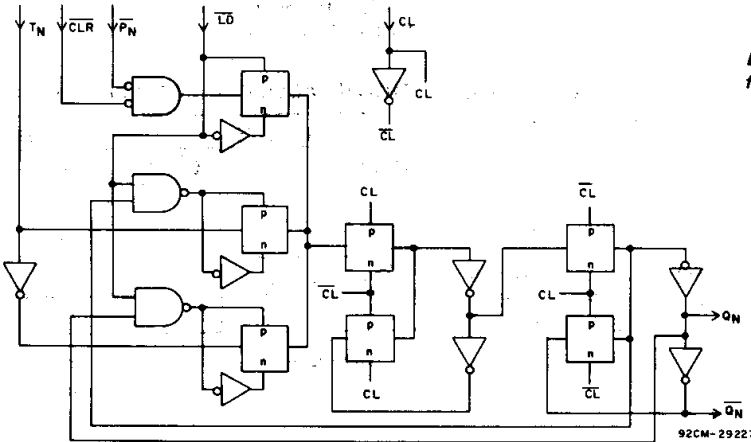
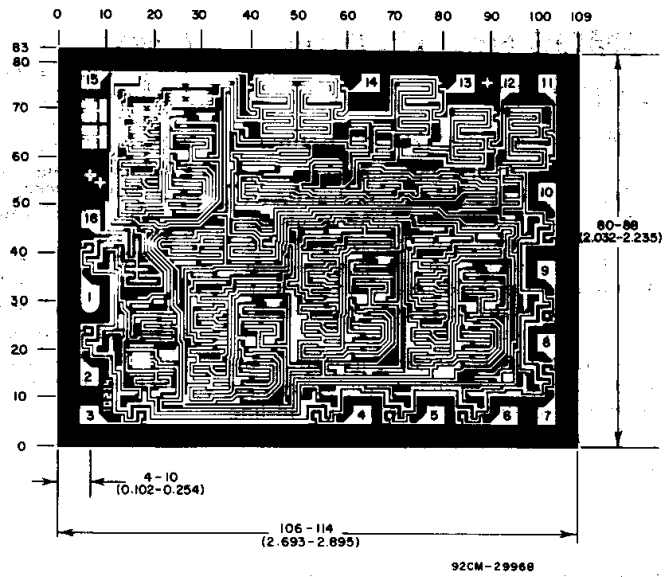


Fig. 17— Detail of flip-flops for CD40162B and CD40163B (synchronous clear).



Dimensions and pad layout for CD40160BH. Dimensions and pad layout for CD40161BH, CD40162BH, and CD40163BH are identical.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

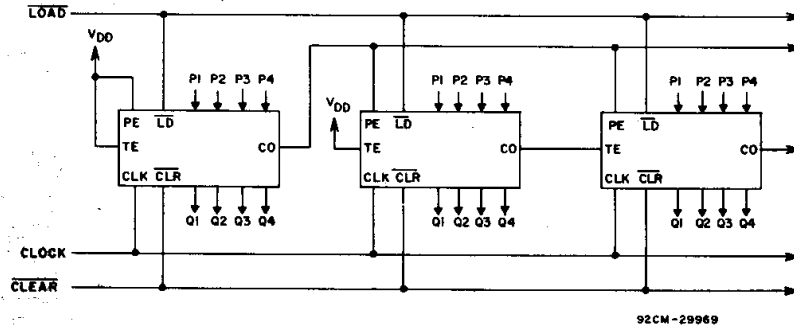


Fig. 18 — Cascaded counter packages in the parallel-clocked mode.

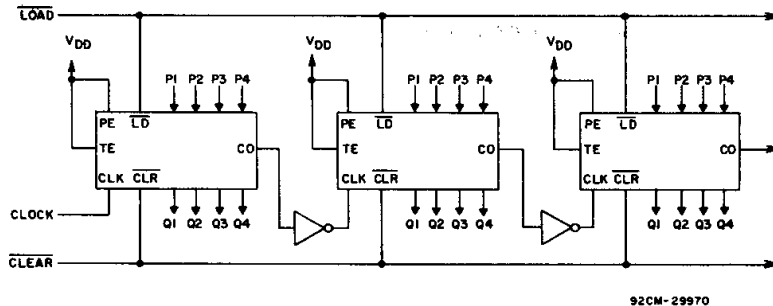


Fig. 19 — Cascaded counter packages in the ripple-clocked mode.

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD40160BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD40160BF3A	Samples
CD40161BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD40161BE	Samples
CD40161BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD40161BE	Samples
CD40161BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD40161BF3A	Samples
CD40161BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40161B	Samples
CD40161BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0161B	Samples
CD40161BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0161B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD40161B, CD40161B-MIL :

- Catalog: [CD40161B](#)

- Military: [CD40161B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40161BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD40161BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40161BNSR	SO	NS	16	2000	367.0	367.0	38.0
CD40161BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.