

NDK

Ordering information for 2560NK, 2560TK series

Please specify p/n as follows:

Series - ppm - Operating Temperature - Symmetry - Frequency

15	-	E	0 to 70 deg C	None	60/40	-	None
20	-	D	-.40 to +85 deg C	I	45/55	-	T
25	-	C	-.10 to 70 deg C	G			
50	-	A	-.20 to 70 deg C	H			
100	-	B					

For example, p/n for 5v, 50ppm, 40/60 symmetry, 0 to 70 deg C, will be

2560NK - A - 50 Mhz

NKAXX
o **50.000m**

p/n for 1.544 Mhz, 3.3v, 25ppm, 45/55 symmetry, -40 to +85 will be

2560TK - C - I - T - 1.544 Mhz

TKCITXX
o **1.544m**

X X is the date code, Year, month (Standard NDK)

Last revision: 4/5/2000



2560TK SERIES

Main Applications: Portable PC, PDA, and PC Cards.

Features:

- Supply voltage 3.3 Volts
- Directly drives C-MOS IC
- Leadless type clock oscillator. Fits highly dense mounting, with light & small demand surface mounting.
Height 1.72mm (max), Weight 0.25g, Occupying area 38mm²
- Highly reliable ceramic package is used so that superior heat-resistance and environmental characteristics are realized.
- IR reflow, automatic mounting are applicable.
- Frequency range: 1.5 MHz to 125 MHz.
- Stand-by function for output: Tri-state output.
- Static electricity proof package: tape & reel.

2560TK SERIES

Model	2560TK			
Item	C-MOS			
Output Level	C-MOS			
Frequency Range (MHz)	1.5 ≤ F ≤ 32	32 < F ≤ 50	50 < F ≤ 67	67 ≤ F ≤ 125
Frequency Stability (ppm)*	± 20, ± 25, ± 50, ± 100			
Operating Temperature (deg C)	0° to +70°C, -10 to +70, -20 to +70, -40 to +85			
Supply Voltage (V _{DD})	+3.3V ± 0.3V			
Current Consumption (mA) @ 3.3 V, 25 Deg C.	10 (max)	15 (max)	18 (max)	45 (max)
V _{OL} max / V _{OL} min	0.1 V _{DD} /0.9V _{DD} . I _{OL} = 2mA I _{OH} = -2mA			
Tr max / Tf max (ns)	6/6 (0.1V _{DD} - 0.9 V _{DD})			
Duty Cycle (%)	45 - 55 (at +1/2 V _{DD})		40 - 60 (at +1/2 V _{DD})	
Fanout (gate)	15 (pF)			
Stand-by Function	Yes, Tri-state			

* Not all stabilities available at -20 to +70 and - 40 to +85 deg C.

Jitter: 3.5 ps RMS max., 3 ps RMS typical.

PAD NO.	Connection
#1	STAND-BY
#2	GND
#3	OUTPUT
#4	VDD

#1 pin input	#3 pin output
H level (+2.2 V min) or open	Operating
L level (+0.8V max)	High Impedance

