Arm® Cortex®-M7 32-bit 550 MHz MCU, 1 MB flash, 564 KB RAM, Ethernet, USB, 3x FD-CAN, Graphics, 2x 16-bit ADCs, crypto/hash

Datasheet - production data

Features

Includes ST state-of-the-art patented technology

Core

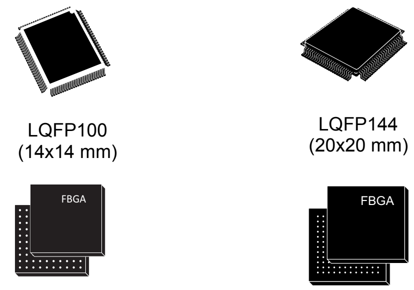
- 32-bit Arm® Cortex®-M7 CPU with DP-FPU, L1 cache: 32-Kbyte data cache and 32-Kbyte instruction cache allowing 0-wait state execution from embedded flash memory and external memories, frequency up to 550 MHz, MPU, 1177 DMIPS/2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions

Memories

- 1 Mbyte of embedded flash memory with ECC
- SRAM: total 564 Kbytes all with ECC, including 128 Kbytes of data TCM RAM for critical real-time data + 432 Kbytes of system RAM (up to 256 Kbytes can remap on instruction TCM RAM for critical real time instructions) + 4 Kbytes of backup SRAM (available in the lowest-power modes)
- Flexible external memory controller with up to 16-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND memories
- 2 x Octo-SPI interface with XiP and on-the-fly decryption support
- 2 x SD/SDIO/MMC interface
- Bootloader with security services support (SFI and SB-SFU)

Graphics

- Chrom-ART Accelerator graphical hardware accelerator enabling enhanced graphical user interface to reduce CPU load
- LCD-TFT controller supporting up to XGA resolution



Clock, reset and supply management

- 1.62 V to 3.6 V application supply and I/O
- POR, PDR, PVD and BOR
- Dedicated USB power
- Embedded LDO regulator
- Internal oscillators: 64 MHz HSI, 48 MHz HSI48, 4 MHz CSI, 32 kHz LSI
- External oscillators: 4-50 MHz HSE, 32.768 kHz LSE

Low power

- Sleep, Stop and Standby modes
- V_{BAT} supply for RTC, 32×32-bit backup registers

Analog

- 2×16-bit ADC, up to 3.6 MSPS in 16-bit: up to 18 channels and 7.2 MSPS in double-interleaved mode
- 1 x 12-bit ADC, up to 5 MSPS in 12-bit, up to 12 channels
- 2 x comparators
- 2 x operational amplifier GBW = 8 MHz
- 2× 12-bit D/A converters

Digital filters for sigma delta modulator (DFSDM)

- 8 channels/4 filters

4 DMA controllers to offload the CPU

- 1 × MDMA with linked list support
- 2 × dual-port DMAs with FIFO
- 1 × basic DMA with request router capabilities

24 timers

- Seventeen 16-bit (including 5 x low power 16-bit timer available in stop mode) and four 32-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- 2x watchdogs, 1x SysTick timer

Debug mode

- SWD and JTAG interfaces
- 2-Kbyte embedded trace buffer

Up to 114 I/O ports with interrupt capability

Up to 35 communication interfaces

- Up to 5 × I2C FM+ interfaces (SMBus/PMBus™)
- Up to 5 USARTs/5 UARTs (ISO7816 interface, LIN, IrDA, modem control) and 1 x LPUART
- Up to 6 SPIs with 4 with muxed duplex I2S for audio class accuracy via internal audio PLL or external clock and up to 5 x SPI (from 5 x USART when configured in synchronous mode)
- 2x SAI (serial audio interface)
- 1× FD/TT-CAN and 2x FD-CAN
- 8- to 14-bit camera interface
- 16-bit parallel slave synchronous interface
- SPDIF-IN interface
- HDMI-CEC
- Ethernet MAC interface with DMA controller
- USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip FS PHY and ULPI for external HS PHY
- SWPMI single-wire protocol master I/F
- MDIO slave interface

Mathematical acceleration

- CORDIC for trigonometric functions acceleration
- FMAC: Filter mathematical accelerator

Digital temperature sensor

Cryptographic/HASH acceleration

- AES 128, 192, 256, TDES, HASH (MD5, SHA-1, SHA-2), HMAC
- 2x OTFDEC AES-128 in CTR mode for Octo-SPI memory encryption/decryption

True random number generator

CRC calculation unit

RTC with subsecond accuracy and hardware calendar

ROP, PC-ROP, tamper detection, secure firmware upgrade support

96-bit unique ID

All packages are ECOPACK2 compliant

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1 Introduction

This document provides information on STM32H733xG microcontrollers, such as description, functional overview, pin assignment and definition, packaging, and ordering information.

This document should be read in conjunction with the STM32H733xG reference manual (RM0468), available from the STMicroelectronics website *www.st.com*.

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32H733 errata sheet (ES0491) available on the STMicroelectronics website *www.st.com*.

For information on the Arm®[a] Cortex®-M7 core, refer to the Cortex®-M7 Technical Reference Manual, available from the http://www.arm.com website.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Description

STM32H733xG devices are based on the high-performance Arm® Cortex®-M7 32-bit RISC core operating at up to 550 MHz. The Cortex® -M7 core features a floating-point unit (FPU) which supports Arm® double-precision (IEEE 754 compliant) and single-precision data-processing instructions and data types. The Cortex -M7 core includes 32 Kbytes of instruction cache and 32 Kbytes of data cache. STM32H733xG devices support a full set of DSP instructions and a memory protection unit (MPU) to enhance application security.

STM32H733xG devices incorporate high-speed embedded memories with 1 Mbyte of flash memory, up to 564 Kbytes of RAM (including 192 Kbytes that can be shared between ITCM and AXI, plus 64 Kbytes exclusively ITCM, plus 128 Kbytes exclusively AXI, 128 Kbyte DTCM, 48 Kbytes AHB and 4 Kbytes of backup RAM), as well as an extensive range of enhanced I/Os and peripherals connected to APB buses, AHB buses, 2x32-bit multi-AHB bus matrix and a multilayer AXI interconnect supporting internal and external memory access. To improve application robustness, all memories feature error code correction (one error correction, two error detections).

The devices embed peripherals allowing mathematical/arithmetic function acceleration (CORDIC coprocessor for trigonometric functions and FMAC unit for filter functions). All the devices offer three ADCs, two DACs, two operational amplifiers, two ultra-low-power comparators, a low-power RTC, four general-purpose 32-bit timers, 12 general-purpose 16-bit timers including two PWM timers for motor control, five low-power timers, a true random number generator (RNG), and a cryptographic acceleration cell, and a HASH processor. The devices support four digital filters for external sigma-delta modulators (DFSDM). They also feature standard and advanced communication interfaces.

- Standard peripherals
  - Five I^2Cs
  - Five USARTs, five UARTs, and one LPUART
  - Six SPIs, four I^2Ss. To achieve audio class accuracy, the I^2S peripherals can be clocked by a dedicated internal audio PLL or by an external clock to allow synchronization (note that the five USARTs also provide SPI slave capability).
  - Two SAI serial audio interfaces
  - One SPDIFRX interface with four inputs
  - One SWPMI (Single Wire Protocol Master Interface)
  - Management Data Input/Output (MDIO) slaves
  - Two SDMMC interfaces
  - A USB OTG high-speed interface with full-speed capability (with the ULPI)
  - Two FDCANs plus one TT-FDCAN interface
  - An Ethernet interface
  - Chrom-ART Accelerator
  - HDMI-CEC

- Advanced peripherals including
  - A flexible memory control (FMC) interface
  - Two Octo-SPI memory interfaces with on-the-fly decryption (OTFDEC)
  - A camera interface for CMOS sensors
  - An LCD-TFT display controller

Refer to *Table 1: STM32H733xG features and peripheral counts* for the list of peripherals available on each part number.

STM32H733xG devices operate in the –40 to +85 °C ambient temperature range from a 1.62 to 3.6 V power supply. The supply voltage can drop down to 1.62 V by using an external power supervisor (see *Section 3.8.2: Power supply supervisor)* and connecting the PDR_ON pin to V_{SS}. Otherwise, the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.

Dedicated supply inputs for USB are available to allow a greater power supply choice.

A comprehensive set of power-saving modes allows the design of low-power applications.

STM32H733xG devices are offered in several packages ranging from 100 to 144 pins/balls. The set of included peripherals changes with the device chosen.

These features make STM32H733xG microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile applications, Internet of Things
- Wearable devices: smart watches.

Figure 1 shows the device block diagram.

Figure 1. STM32H733xG block diagram

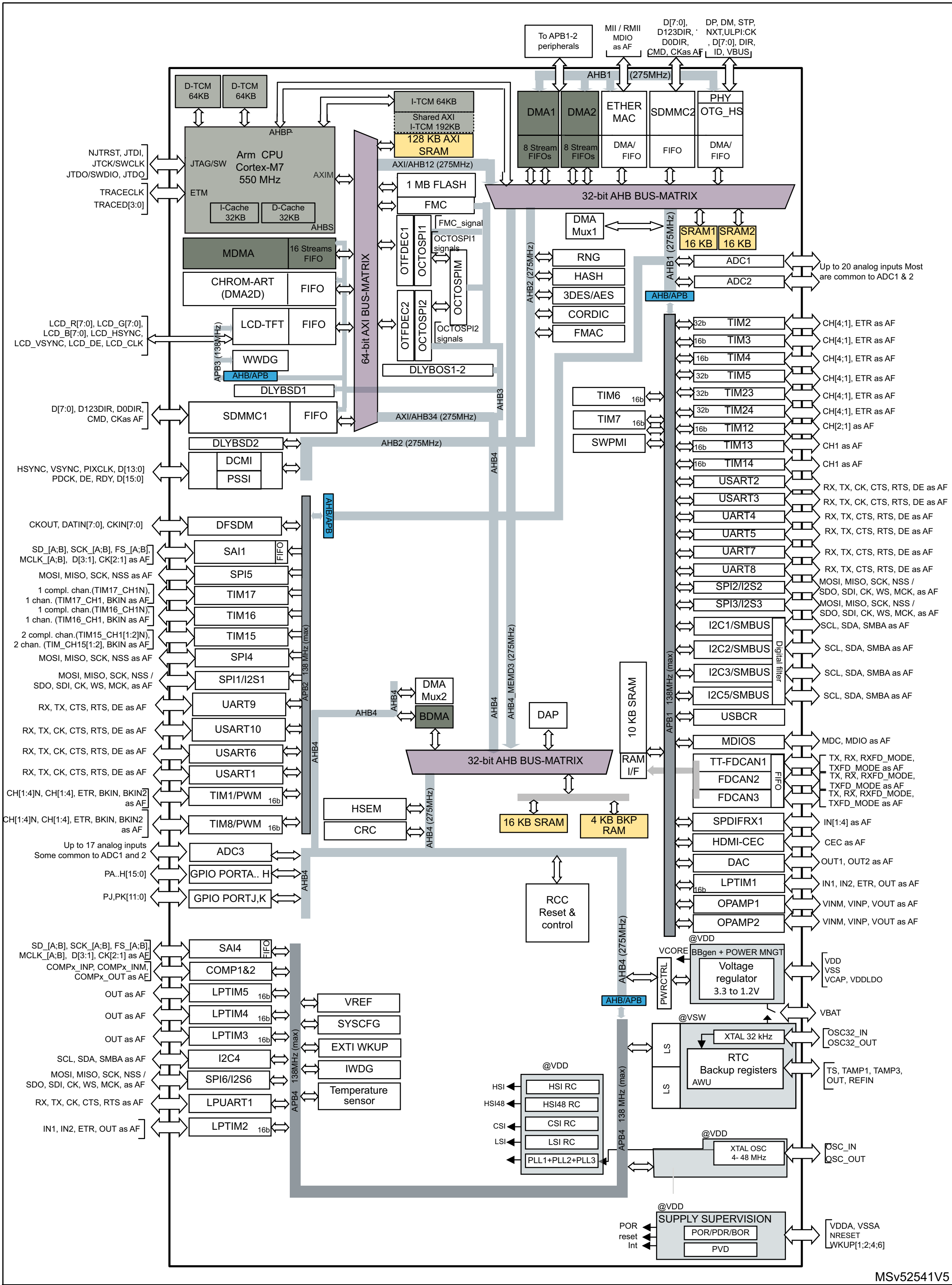


Table 1. STM32H733xG features and peripheral counts

Peripherals		STM32H733VGH	STM32H733VGT	STM32H733ZGT	STM32H733ZGI
Flash memory (Kbytes)		1024	1024	1024	1024
SRAM (Kbytes)	SRAM mapped onto AXI bus	128			
	SRAM1 (D2 domain)	16			
	SRAM2 (D2 domain)	16			
	SRAM4 (D3 domain)	16			
RAM shared between ITCM and AXI (Kbytes)		192			
TCM RAM (Kbytes)	ITCM RAM (instruction)	64			
	DTCM RAM (data)	128			
Backup SRAM (Kbytes)		4			
FMC	Interface	1			
	NOR flash memory/RAM controller	-	-	yes	yes
	Multiplexed I/O NOR flash memory	yes	yes	yes	yes
	16-bit NAND flash memory	yes	yes	yes	yes
	16-bit SDRAM controller	-	-	yes	yes
GPIO		80	80	112	114
Octo-SPI interface		1	1	2	2
OTFDEC		yes			
CORDIC		yes			
FMAC		yes			
Timers	General purpose 32 bits	4	4	4	4
	General purpose 16 bits	10	10	10	10
	Advanced control (PWM)	2	2	2	2
	Basic	2	2	2	2
	Low-power	5	5	5	5
	RTC	1	1	1	1
	Window watchdog / independent watchdog	2	2	2	2
Wakeup pins		4	4	4	4
Tamper pins		2	2	2	2
Random number generator		yes			

Table 1. STM32H733xG features and peripheral counts (continued)

Peripherals		STM32H733VGH	STM32H733VGT	STM32H733ZGT	STM32H733ZGI
Cryptographic accelerator		yes			
Communication interfaces	SPI / I2S	5/4	5/4	6/4	6/4
	I2C	5	5	5	5
	USART/UART/ LPUART	5/5/1	5/5/1	5/5/1	5/5/1
	SAI/PDM	2/2(1)	2/2(1)	2/2	2/2
	SPDIFRX	1			
	HDMI-CEC	1			
	SWPMI	1			
	MDIO	/1			
	SDMMC	2			
	FDCAN/TT-FDCAN	2/1	2/1	2/1	2/1
	USB [OTG_HS(ULPI)/FS(PHY)]	1 [1/1]	1 [1/1]	1 [1/1]	1 [1/1]
	Ethernet [MII/RMII]	1 [0/1]	1 [0/1]	1 [0/1]	1 [1/1]
Camera interface/PSSI		yes			
LCD-TFT		yes	yes	yes	yes
Chrom-ART Accelerator (DMA2D)		yes			
16-bit ADCs	Number of ADCs	2			
	Number of direct channelsADC1/ADC2	2/2	0	0	2/2
	Number of fast channels ADC1/ADC2	3/2	3/2	4/3	4/3
	Number of slow channels ADC1/ADC2	9/8	11/10	12/11	12/11
12-bit ADCs	Number of ADCs	1			
	Number of direct channels	2	2	2	2
	Number of fast channels	6	2	6	6
	Number of slow channels	9	0	4	9
12-bit DAC	Present in IC	yes			
	Number of channels	2			
	Comparators	2			
	Operational amplifiers	2			
DFSDM	Present in IC	yes			
Maximum CPU frequency		550 MHz			
USB separate supply pad		yes	-	yes	yes

Table 1. STM32H733xG features and peripheral counts (continued)

Peripherals		STM32H733VGH	STM32H733VGT	STM32H733ZGT	STM32H733ZGI
USB internal regulator		-	-	-	-
LDO		yes			
SMPS step-down converter		-	-	-	-
Operating voltage		1.62 to 3.6 V	1.71 to 3.6 V	1.62 to 3.6 V	
Operating temperatures	Ambient temperature	-40°C to +85°C			
	Junction temperature	-40°C to +125°C			
Package		TFBGA100	LQFP100	LQFP144	UFBGA144

1. For limitations on peripheral features depending on packages, check the available pins/balls in *Table 8: STM32H733 pin alternate functions*.

3 Functional overview

3.1 Arm® Cortex®-M7 with FPU

The Arm® Cortex®-M7 with double-precision FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and optimized power consumption, while delivering outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard architecture with L1 caches (32 Kbytes of I-cache and 32 Kbytes of D-cache)
- 64-bit AXI interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The following memory interfaces are supported:

- Separate Instruction and Data buses (Harvard Architecture) to optimize CPU latency
- Tightly Coupled Memory (TCM) interface designed for fast and deterministic SRAM accesses
- AXI Bus interface to optimize Burst transfers
- Dedicated low-latency AHB-Lite peripheral bus (AHBP) to connect to peripherals.

The processor supports a set of DSP instructions, which allow efficient signal processing and complex algorithm execution.

It also supports single and double precision FPU (floating-point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

Figure 1 shows the general block diagram of the STM32H733xG family.

3.2 Memory protection unit (MPU)

The memory protection unit (MPU) manages the CPU access rights and the attributes of the system resources. It has to be programmed and enabled before use. Its main purposes are to prevent an untrusted user program to accidentally corrupt data used by the OS and/or by a privileged task, but also to protect data processes or read-protect memory regions.

The MPU defines access rules for privileged accesses and user program accesses. It allows defining up to 16 protected regions that can in turn be divided into up to eight independent subregions, where region address, size, and attributes can be configured. The protection area ranges from 32 bytes to 4 Gbytes of addressable memory.

When an unauthorized access is performed, a memory management exception is generated.

3.3 Memories

3.3.1 Embedded flash memory

The STM32H733xG devices embed 1 Mbyte of flash memory that can be used for storing programs and data.

The flash memory is organized as 266-bit flash words memory that can be used for storing both code and data constants. Each word consists of:

- one flash word (eight words, 32 bytes, or 256 bits)
- 10 ECC bits (single-error correction and double-error detection).

The flash memory is organized as follows:

- 1 Mbyte of user flash memory block containing eight user sectors of 128 Kbytes (4 K flash memory words)
- 128 Kbytes of system flash memory from which the device can boot
- 2 Kbytes (64 flash words) of user option bytes for user configuration

3.3.2 Embedded SRAM

All devices feature:

- from 128 to 320 Kbytes of AXI-SRAM mapped onto the AXI bus on D1 domain
- SRAM1 mapped on D2 domain: 16 Kbytes
- SRAM2 mapped on D2 domain: 16 Kbytes
- SRAM4 mapped on D3 domain: 16 Kbytes
- 4 Kbytes of backup SRAM

  The content of this area is protected against possible unwanted write accesses, and can be retained in Standby or V_{BAT} mode.
- RAM mapped to TCM interface (ITCM and DTCM):

  Both ITCM and DTCM RAMs are zero wait state memories. They can be accessed either from the CPU or the MDMA (even in Sleep mode) through a specific AHB slave of the Cortex®-M7CPU(AHBSAHBP):
  - 64 to 256 Kbytes of ITCM-RAM (instruction RAM)

    This RAM is connected to an ITCM 64-bit interface designed for execution of critical real-time routines by the CPU.
  - 128 Kbytes of DTCM-RAM (2x 64-Kbyte DTCM-RAMs on 2x32-bit DTCM ports)

    The DTCM-RAM could be used for critical real-time data, such as interrupt service routines or stack/heap memory. Both DTCM-RAMs can be used in parallel (for load/store operations) thanks to the Cortex®-M7 dual issue capability.

  The MDMA can be used to load code or data in ITCM or DTCM RAMs. As reflected above, 192 Kbyte of RAM can be used either for AXI SRAM or ITCM, with a 64Kbyte granularity.

Error code correction (ECC)

Over the product lifetime, and/or due to external events such as radiations, invalid bits in memories may occur. They can be detected and corrected by ECC. This is an expected behavior that has to be managed at final-application software level in order to ensure data integrity through ECC algorithms implementation.

SRAM data are protected by ECC:

- 7 ECC bits are added per 32-bit word.
- 8 ECC bits are added per 64-bit word for AXI-SRAM and ITCM-RAM.

The ECC mechanism is based on the SECDED algorithm. It supports single-error correction and double-error detection.

3.4 Secure access mode

In addition to other typical memory protection mechanism (RDP, PCROP), STM32H733xG devices introduce the Secure access mode, a new enhanced security feature. This mode allows developing user-defined secure services by ensuring, on the one hand code and data protection and on the other hand code safe execution.

Two types of secure services are available:

- STMicroelectronics Root Secure Services:

  These services are embedded in System memory. They provide a secure solution for firmware and third-party modules installation. These services rely on cryptographic algorithms based on a device unique private key.
- User-defined secure services:

  These services are embedded in user flash memory. Examples of user secure services are proprietary user firmware update solution, secure flash integrity check or any other sensitive applications that require a high level of protection.

  The secure firmware is embedded in specific user flash memory areas configured through option bytes.

Secure services are executed just after a reset and preempt all other applications to guarantee protected and safe execution. Once executed, the corresponding code and data are no more accessible.

The above secure services is activated for the next reset exits through an option bit.

3.5 Boot modes

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF, which includes:

- All flash address space
- All RAM address space: ITCM, DTCM RAMs and SRAMs
- The system memory bootloader

The bootloader is located in nonuser system memory. It is used to reprogram the flash memory through a serial interface (USART, I2C, SPI, FDCAN, USB-DFU). Refer to application note AN2606 “*STM32 microcontroller system memory Boot mode”* for details.

3.6 CORDIC coprocessor (CORDIC)

The CORDIC coprocessor provides hardware acceleration of certain mathematical functions, notably trigonometric, commonly used in motor control, metering, signal processing and many other applications.

It speeds up the calculation of these functions compared to a software implementation, allowing a lower operating frequency, or freeing up processor cycles in order to perform other tasks.

The filter mathematical accelerator unit performs arithmetic operations on vectors. It comprises a multiplier/accumulator (MAC) unit, together with address generation logic, which allows it to index vector elements held in local memory.

The unit includes support for circular buffers on input and output, which allows digital filters to be implemented. Both finite and infinite impulse response filters can be realized.

The unit allows frequent or lengthy filtering operations to be offloaded from the CPU, freeing up the processor for other tasks. In many cases it can accelerate such calculations compared to a software implementation, resulting in a speed-up of time critical tasks.

CORDIC features

- 24-bit CORDIC rotation engine
- Circular and Hyperbolic modes
- Rotation and Vectoring modes
- Functions: Sine, Cosine, Sinh, Cosh, Atan, Atan2, Atanh, Modulus, Square root, Natural logarithm
- Programmable precision up to 20-bit
- Fast convergence: 4 bits per clock cycle
- Supports 16-bit and 32-bit fixed point input and output formats
- Low latency AHB slave interface
- Results can be read as soon as ready without polling or interrupt
- DMA read and write channels

3.7 Filter mathematical accelerator (FMAC)

The filter mathematical accelerator unit performs arithmetic operations on vectors. It comprises a multiplier/accumulator (MAC) unit, together with address generation logic, which allows it to index vector elements held in local memory.

The unit includes support for circular buffers on input and output, which allows digital filters to be implemented. Both finite and infinite impulse response filters can be realized.

The unit allows frequent or lengthy filtering operations to be offloaded from the CPU, freeing up the processor for other tasks. In many cases it can accelerate such calculations compared to a software implementation, resulting in a speed-up of time critical tasks.

FMAC features

- 16 x 16-bit multiplier
- 24+2-bit accumulator with addition and subtraction
- 16-bit input and output data
- 256 x 16-bit local memory
- Up to three areas can be defined in memory for data buffers (two inputs, one output), defined by programmable base address pointers and associated size registers
- Input and output sample buffers can be circular
- Buffer “watermark” feature reduces overhead in interrupt mode
- Filter functions: FIR, IIR (direct form 1)
- AHB slave interface
- DMA read and write data channels

3.8 Power supply management

3.8.1 Power supply scheme

STM32H733xG power supply voltages are the following:

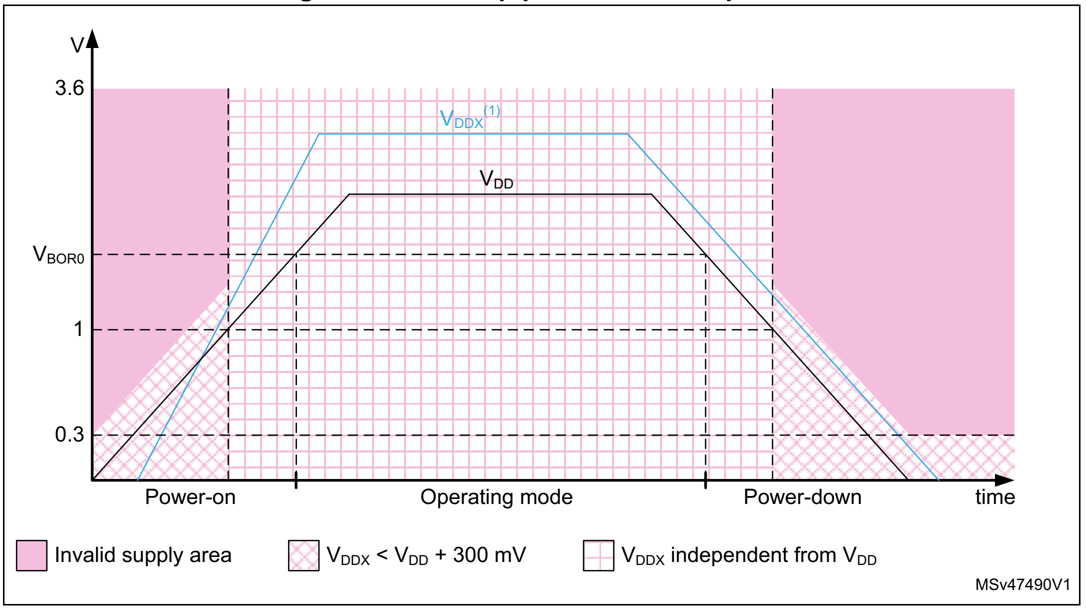
- V_{DD} = 1.62 to 3.6 V: external power supply for I/Os, provided externally through V_{DD} pins.
- V_{DDLDO} = 1.62 to 3.6 V: supply voltage for the internal regulator supplying V_{CORE}
- V_{DDA} = 1.62 to 3.6 V: external analog power supplies for ADC, DAC, COMP and OPAMP.
- $V_{DD33USB}$: allows the support of a VDD supply different from 3.3 V while powering the USB transceiver with 3.3V on $V_{DD33USB}$.
- V_{BAT} = 1.2 to 3.6 V: power supply for the V_{SW} domain when V_{DD} is not present.
- V_{CAP}: V_{CORE} supply voltage, which values depend on voltage scaling (1.0 V, 1.1 V, 1.2 V or 1.35 V). They are configured through VOS bits in PWR_D3CR register. The V_{CORE} domain is split into the following power domains that can be independently switch off.
  – D1 domain containing some peripherals and the Cortex®-M7 core
  – D2 domain containing a large part of the peripherals
  – D3 domain containing some peripherals and the system control

During power-up and power-down phases, the following power sequence requirements must be respected (see *Figure 2*):

- When V_{DD} is below V_{DDmin}, other power supplies (V_{DDA}, $V_{DD33USB}$) must remain below V_{DD} + 300 mV.
- When V_{DD} is above V_{DDmin}, all power supplies are independent.

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the microcontroller remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 2. Power-up/power-down sequence



1. V_{DDx} refers to any power supply among V_{DDA}, $V_{DD33USB}$.

3.8.2 Power supply supervisor

The devices have an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a brownout reset (BOR) circuitry:

- Power-on reset (POR)

  The POR supervisor monitors V_{DD} power supply and compares it to a fixed threshold. The devices remain in reset mode when V_{DD} is below this threshold,
- Power-down reset (PDR)

  The PDR supervisor monitors V_{DD} power supply. A reset is generated when V_{DD} drops below a fixed threshold.

  The PDR supervisor can be enabled/disabled through PDR_ON pin.
- Brownout reset (BOR)

  The BOR supervisor monitors V_{DD} power supply. Three BOR thresholds (from 2.1 to 2.7 V) can be configured through option bytes. A reset is generated when V_{DD} drops below this threshold.

3.8.3 Voltage regulator

The same voltage regulator supplies the three power domains (D1, D2, and D3). D1 and D2 can be independently switched off.

Voltage regulator output can be adjusted according to application needs through six power supply levels:

- Run mode (VOS0 to VOS3)
  - Scale 0: boosted performance
  - Scale 1: high performance
  - Scale 2: medium performance and consumption
  - Scale 3: optimized performance and low-power consumption
- Stop mode (SVOS3 to SVOS5)
  - Scale 3: peripheral with wake-up from Stop mode capabilities (UART, SPI, I2C, LPTIM) are operational
  - Scale 4 and 5 where the peripheral with wake-up from Stop mode is disabled. The peripheral functionality is disabled but wake-up from Stop mode is possible through GPIO or asynchronous interrupt.

3.9 Low-power strategy

There are several ways to reduce power consumption on STM32H733xG:

- Decrease the dynamic power consumption by slowing down the system clocks even in Run mode and by individually clock gating the peripherals that are not used.
- Save power when the CPU is idle, by selecting among the available low-power modes according to the user application needs. This allows the best compromise between short startup time and low power consumption to be achieved, according to the available wake-up sources.

The devices feature several low-power modes:

- CSleep (CPU clock stopped)
- CStop (CPU subsystem clock stopped)
- DStop (Domain bus matrix clock stopped)
- Stop (system clock stopped)
- DStandby (Domain powered down)
- Standby (system powered down)

CSleep and CStop low-power modes are entered by the MCU when executing the WFI (Wait for Interrupt) or WFE (Wait for Event) instructions, or when the SLEEPONEXIT bit of the Cortex®-Mx core is set after returning from an interrupt service routine.

A domain can enter low-power mode (DStop or DStandby) when the processor, its subsystem, and the peripherals allocated in the domain enter low-power mode.

If part of the domain is not in low-power mode, the domain remains in the current mode.

Finally, the system can enter Stop or Standby when all EXTI wake-up sources are cleared and the power domains are in DStop or DStandby mode.

Table 2. System versus domain low-power mode

System power mode	D1 domain power mode	D2 domain power mode	D3 domain power mode
Run	DRun/DStop/DStandby	DRun/DStop/DStandby	DRun
Stop	DStop/DStandby	DStop/DStandby	DStop
Standby	DStandby	DStandby	DStandby

3.10 Reset and clock controller (RCC)

The clock and reset controller is located in D3 domain. The RCC manages the generation of all the clocks, as well as the clock gating and the control of the system and peripheral resets. It provides a high flexibility in the choice of clock sources and allows clock ratios to be applied to improve the power consumption. In addition, on some communication peripherals that are capable to work with two different clock domains (either a bus interface clock or a kernel peripheral clock), thus the system frequency can be changed without modifying the baud rate.

3.10.1 Clock management

The devices embed four internal oscillators, two oscillators with external crystal or resonator, two internal oscillators with fast startup time and three PLLs.

The RCC receives the following clock source inputs:

- Internal oscillators:
  - 64 MHz HSI clock
  - 48 MHz RC oscillator
  - 4 MHz CSI clock
  - 32 kHz LSI clock
- External oscillators:
  - HSE clock: 4-50 MHz (generated from an external source) or 4-48 MHz(generated from a crystal/ceramic resonator)
  - LSE clock: 32.768 kHz

The RCC provides three PLLs: one for system clock, two for kernel clocks.

The system starts on the HSI clock. The user application can then select the clock configuration.

3.10.2 System reset sources

Power-on reset initializes all registers while system reset reinitializes the system except for the debug, part of the RCC and power controller status registers, as well as the backup power domain.

A system reset is generated in the following cases:

- Power-on reset (pwr_por_rst)
- Brownout reset
- Low level on NRST pin (external reset)
- Window watchdog
- Independent watchdog
- Software reset
- Low-power mode security reset
- Exit from Standby

3.11 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

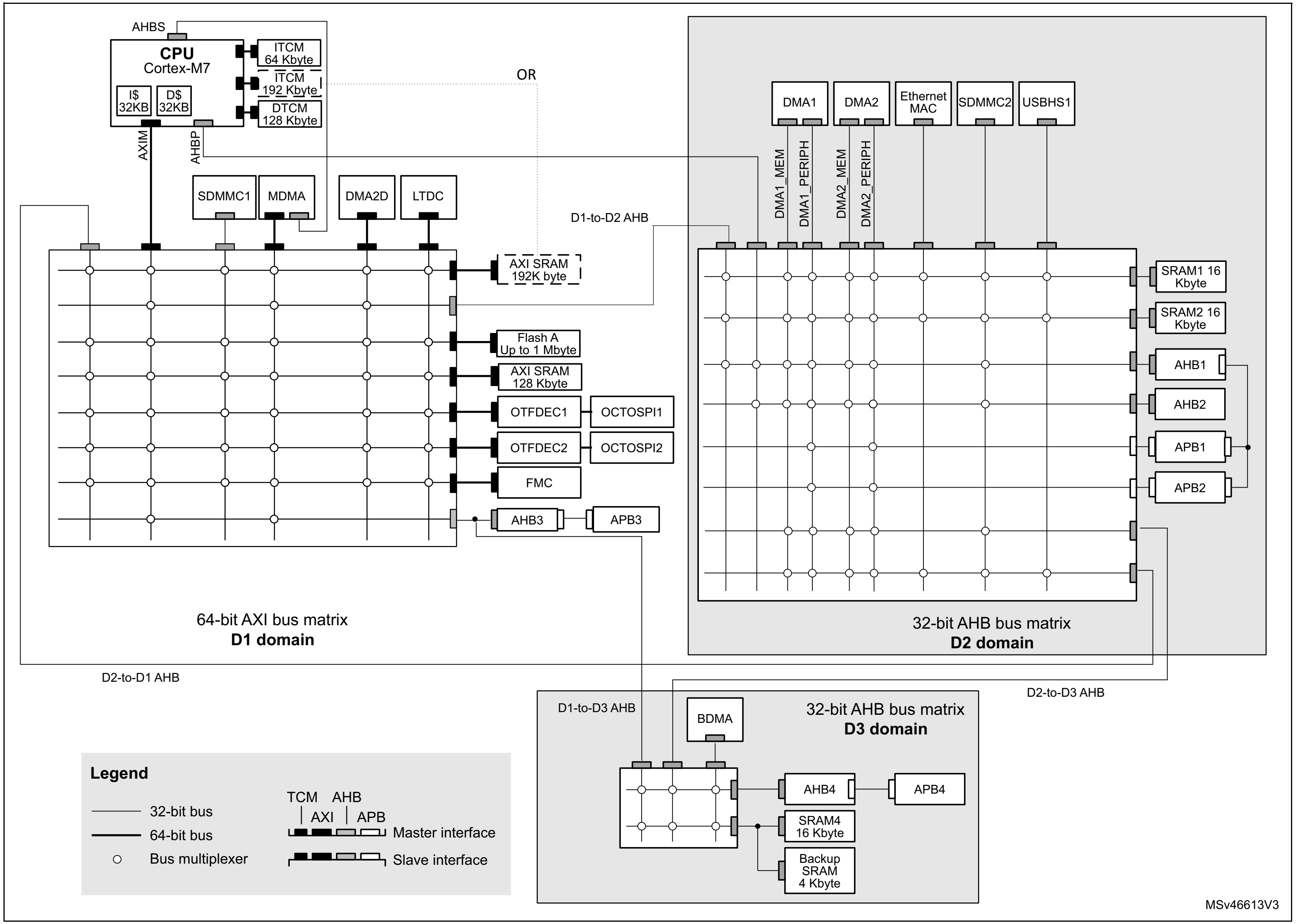
After reset, all GPIOs (except debug pins) are in Analog mode to reduce power consumption (refer to GPIOs register reset values in the device reference manual).

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.12 Bus-interconnect matrix

The devices feature an AXI bus matrix, two AHB bus matrices and bus bridges that allow the interconnection of bus masters with bus slaves (see *Figure 3*).

Figure 3. STM32H733xG bus matrix



3.13 DMA controllers

The devices feature four DMA instances and a DMA request router to unload CPU activity:

- A master direct memory access (MDMA)

  The MDMA is a high-speed DMA controller, which is in charge of all types of memory transfers (peripheral to memory, memory to memory, memory to peripheral), without any CPU action. It features a master AXI interface and a dedicated AHB interface to access Cortex®-M7 TCM memories.

  The MDMA is located in D1 domain. It is able to interface with the other DMA controllers located in D2 domain to extend the standard DMA capabilities, or can manage peripheral DMA requests directly.

  Each of the 16 channels can perform single block transfers, repeated block transfers and linked list transfers.
- Two dual-port DMAs (DMA1, DMA2) located in D2 domain, with FIFO and request router capabilities.
- One basic DMA (BDMA) located in D3 domain, with request router capabilities.
- A DMA request multiplexer (DMAMUX)

  The DMA request router could be considered as an extension of the DMA controller. It routes the DMA peripheral requests to the DMA controller itself. This allowing managing the DMA requests with a high flexibility, maximizing the number of DMA requests that run concurrently, as well as generating DMA requests from peripheral output trigger or DMA event.

3.14 Chrom-ART Accelerator (DMA2D)

The Chrom-ART Accelerator (DMA2D) is a specialized DMA dedicated to image manipulation. It can perform the following operations:

- Filling a part or the whole of a destination image with a specific color
- Copying a part or the whole of a source image into a part or the whole of a destination image
- Copying a part or the whole of a source image into a part or the whole of a destination image with a pixel format conversion
- Blending a part and/or two complete source images with different pixel format and copy the result into a part or the whole of a destination image with a different color format.
- All the classical color coding schemes are supported from 4-bit up to 32-bit per pixel with indexed or direct color mode, including block based YCbCr to handle JPEG decoder output.
- The DMA2D has its own dedicated memories for CLUTs (color look-up tables).

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automated and are running independently from the CPU or the DMAs.

3.15 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller, which is able to manage 16 priority levels, and handle up to 140 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor context automatically saved on interrupt entry, and restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.16 Extended interrupt and event controller (EXTI)

The EXTI controller performs interrupt and event management. In addition, it can wake up the processor, power domains and/or D3 domain from Stop mode.

The EXTI handles up to 80 independent event/interrupt lines split as 26 configurable events and 54 direct events.

Configurable events have dedicated pending flags, active edge selection, and software trigger capable.

Direct events provide interrupts or events from peripherals having a status flag.

3.17 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a programmable polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.18 Flexible memory controller (FMC)

The FMC controller main features are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR flash memory/OneNAND flash memory
  - PSRAM (four memory banks)
  - NAND flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-,16-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is the FMC kernel clock divided by 2.

3.19 Octo-SPI memory interface (OCTOSPI)

The OCTOSPI is a specialized communication interface targeting single, dual, quad, or octal SPI memories. The STM32H733xG embeds two separate Octo-SPI interfaces.

Each OCTOSPI instance supports single/dual/quad/octal SPI formats. multiplexing of single/dual/quad/octal SPI over the same bus can be achieved using the integrated Octo-SPI I/O manager (OCTOSPIM).

The OCTOSPI can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the OCTOSPI registers
- Status-polling mode: the external memory status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external memory is memory mapped and it is seen by the system as if it was an internal memory supporting both read and write operations.

The OCTOSPI supports two frame formats supported by most external serial memories such as serial PSRAMs, serial NAND and serial NOR flash memories, Hyper RAMs and Hyper flash memories.

Multichip package (MCP) combining any of the above mentioned memory types can also be supported.

- The classical frame format with the command, address, alternate byte, dummy cycles, and data phase
- The HyperBus™ frame format.

3.20 Analog-to-digital converters (ADCs)

STM32H733xG devices embed three analog-to-digital converters, two of 16-bit resolution, and the third of 12-bit resolution. The 16-bit resolution ADCs can be configured as 16, 14, 12, 10 or 8 bits. The 12-bit resolution ADC can be configured to 12, 10 or 8 bits.

Each ADC shares up to 20 external channels, performing conversions in Single-shot or Scan mode. In Scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller, thus allowing automatic transfer of ADC converted values to a destination location without any software action.

In addition, an analog watchdog feature can accurately monitor the converted voltage of one, some, or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs can be triggered by any of the TIM1, TIM2, TIM3, TIM4, TIM6, TIM8, TIM15, TIM23, TIM24, and LPTIM1 timers.

3.21 Temperature sensor

STM32H733xG devices embed a temperature sensor that generates a voltage (V_{TS}) that varies linearly with the temperature. This temperature sensor is internally connected to ADC3_IN17. The conversion range is between 1.7 V and 3.6 V. It can measure the device junction temperature ranging from − 40 to +125°C.

The temperature sensor have a good linearity, but it has to be calibrated to obtain a good overall accuracy of the temperature measurement. As the temperature sensor offset varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only. To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, which is accessible in read-only mode.

3.22 Digital temperature sensor (DTS)

STM32H733xG devices embed a sensor that converts the temperature into a square wave the frequency of which is proportional to the temperature. The PCLK or the LSE clock can be used as the reference clock for the measurements. A formula given in the product reference manual allows calculation of the temperature according to the measured frequency stored in the DTS_DR register.

3.23 V_{BAT} operation

The V_{BAT} power domain contains the RTC, the backup registers, and the backup SRAM.

To optimize battery duration, this power domain is supplied by V_{DD} when available or by the voltage applied on VBAT pin (when V_{DD} supply is not present). V_{BAT} power is switched when the PDR detects that V_{DD} dropped below the PDR level.

The voltage on the VBAT pin could be provided by an external battery, a supercapacitor or directly by V_{DD}, in which case, the V_{BAT} mode is not functional.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers, and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When PDR_ON pin is connected to V_{SS} (Internal Reset OFF), the V_{BAT} functionality is no more available and V_{BAT} pin should be connected to VDD.

3.24 Digital-to-analog converters (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel including DMA underrun error detection
- external triggers for conversion
- input voltage reference V_{REF+} or internal VREFBUF reference.

The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

3.25 Ultra-low-power comparators (COMP)

STM32H733xG devices embed two rail-to-rail comparators (COMP1 and COMP2). They feature programmable reference voltage (internal or external), hysteresis, and speed (low speed for low-power) as well as selectable output polarity.

The reference voltage can be one of the following:

- An external I/O
- A DAC output channel
- An internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers, and be combined into a window comparator.

3.26 Operational amplifiers (OPAMP)

STM32H733xG devices embed two rail-to-rail operational amplifiers (OPAMP1 and OPAMP2) with external or internal follower routing and PGA capability.

The operational amplifier main features are:

- PGA with a noninverting gain ranging of 2, 4, 8 or 16 or inverting gain ranging of -1, -3, -7 or -15
- One positive input connected to DAC
- Output connected to internal ADC
- Low input bias current down to 1 nA
- Low input offset voltage down to 1.5 mV
- Gain bandwidth up to 7.3 MHz

The devices embed two operational amplifiers (OPAMP1 and OPAMP2) with two inputs and one output each. These three I/Os can be connected to the external pins, thus enabling any type of external interconnections. The operational amplifiers can be configured internally as a follower, as an amplifier with a noninverting gain ranging from 2 to 16 or with inverting gain ranging from -1 to -15.

3.27 Digital filter for sigma-delta modulators (DFSDM)

The devices embed one DFSDM with four digital filters modules and eight external input serial channels (transceivers) or alternately eight internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in hardware. DFSDM features optional parallel data stream inputs from internal ADC peripherals or microcontroller memory (through DMA/CPU transfers into DFSDM).

DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators). DFSDM digital filter modules perform digital processing according to user-selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 8 multiplexed input digital serial channels:
  - configurable SPI interface to connect various SD modulators
  - configurable Manchester coded 1 wire interface support
  - PDM (Pulse Density Modulation) microphone input support
  - maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - clock output for SD modulators: 0..20 MHz
- alternative inputs from eight internal digital parallel channels (up to 16-bit input resolution):
  - internal sources: ADC data or memory data streams (DMA)
- 4 digital filter modules with adjustable digital signal processing:
  - Sinc^x filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - integrator: oversampling ratio (1..256)
- up to 24-bit output data resolution, signed output data format
- automatic data offset correction (offset stored in register by user)
- continuous or single conversion
- start-of-conversion triggered by:
  - software trigger
  - internal timers
  - external events
  - start-of-conversion synchronously with first digital filter module (DFSDM0)
- analog watchdog feature:
  - low value and high value data threshold registers
  - dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - input from final output data or from selected input digital serial channels
  - continuous monitoring independently from standard conversion
- short circuit detector to detect saturated analog input values (bottom and top range):
  - up to 8-bit counter to detect 1..256 consecutive 0’s or 1’s on serial data stream
  - monitoring continuously each input serial channel
- break signal generation on analog watchdog event or on short circuit detector event

- extremes detector:
  - storage of minimum and maximum values of final conversion data
  - refreshed by software
- DMA capability to read the final conversion data
- interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- “regular” or “injected” conversions:
  - “regular” conversions can be requested at any time or even in Continuous mode without having any impact on the timing of “injected” conversions
  - “injected” conversions for precise timing and with high conversion priority
- Pulse skipper feature to support beamforming applications (delay-line like behavior).

Table 3. DFSDM implementation

DFSDM features	DFSDM1
Number of filters	4
Number of input transceivers/channels	8
Internal ADC parallel input	X
Number of external triggers	16
Regular channel information in identification register	X

3.28 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can achieve a data transfer rate up to 140 Mbyte/s using an 80 MHz pixel clock. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12-, or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports Continuous mode or Snapshot (a single frame) mode
- Capability to automatically crop the image

3.29 PSSI

The PSSI is a generic synchronous 8-/16-bit parallel data input/output slave interface. It allows the transmitter to send a data valid signal to indicate when the data is valid, and the receiver to output a flow control signal to indicate when it is ready to sample the data.

The main PSSI features are:

- Slave mode operation
- 8- or 16-bit parallel data input or output
- 8-word (32-byte) FIFO
- Data enable (DE) alternate function input and Ready (RDY) alternate function output.

When enabled, these signals can either allow the transmitter to indicate when the data is valid or the receiver to indicate when it is ready to sample the data, or both.

The PSSI shares most of its circuitry with the digital camera interface (DCMI). It therefore cannot be used simultaneously with the DCMI.

3.30 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024 x 768) resolution with the following features:

- 2 display layers with dedicated FIFO (64x64-bit)
- Color look-up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to eight input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to four programmable interrupt events
- AXI master interface with burst of 16 words

3.31 True random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

The RNG can be used to construct a nondeterministic random bit generator (NDRBG), as a NIST SP 800-90B compliant entropy source.

The RNG true random number generator has been tested using German BSI statistical tests of AIS-31 (T0 to T8), and NIST SP800-90B statistical test suite.

3.32 Cryptographic acceleration (CRYP and HASH)

The devices embed a cryptographic processor that supports the advanced cryptographic algorithms usually required to ensure confidentiality, authentication, data integrity and non-repudiation when exchanging messages

with a peer:

- Encryption/Decryption
  - DES/TDES (data encryption standard/triple data encryption standard): ECB (electronic codebook) and CBC (cipher block chaining) chaining algorithms, 64-, 128- or 192-bit key
  - AES (advanced encryption standard): ECB, CBC, GCM, CCM, and CTR (counter mode) chaining algorithms, 128, 192 or 256-bit key
- Universal HASH
  - – SHA-1 and SHA-2 (secure HASH algorithms)
  - – MD5
  - – HMAC

The cryptographic accelerator supports DMA request generation.

3.33 On-the-fly decryption engine (OTFDEC)

The embedded OTFDEC decrypts in real-time the encrypted content stored in the external Octo-SPI memories used in Memory-mapped mode.

The OTFDEC uses the AES-128 algorithm in counter mode (CTR).

Code execution on external Octo-SPI memories can be protected against fault injection thanks to

STMicroelectronics enhanced encryption mode (refer to RM0468 for details).

The OTFDEC main features are as follow:

- On-the-fly 128-bit decryption during STM32 Octo-SPI read operations (single or multiple).
  - AES-CTR algorithm with keystream FIFO (depth= 4)
  - Support for any read size
- Up to four independent encrypted regions
  - Region definition granularity: 4096 bytes
  - Region configuration write locking mechanism
  - Two optional decryption modes: execute-only and execute-never
- 128-bit key for each region, two-byte firmware version, and eight-byte application-defined nonce
- Encryption keys confidentiality and integrity protection
  - Write only registers with software locking mechanism
  - Availability of 8-bit CRC as public key information
- Support for STM32 Octo-SPI prefetching mechanism.

3.34 Timers and watchdogs

The devices include two advanced-control timers, twelve general-purpose timers, two basic timers, five low-power timers, two watchdogs and a SysTick timer.

All timer counters can be frozen in Debug mode.

Table 4 compares the features of the advanced-control, general-purpose and basic timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max timer clock (MHz)(1)
Advanced -control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	137.5	275
General purpose	TIM2, TIM5, TIM23, TIM24	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	137.5	275
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	137.5	275
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	137.5	275
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	137.5	275
	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1	137.5	275
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1	137.5	275

Table 4. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max timer clock (MHz)(1)
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	137.5	275
Low-power timer	LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	No	0	No	137.5	275

1. The maximum timer clock is up to 550 MHz depending on theTIMPRE bit in the RCC_CFGR register and D2PRE1/2 bits in RCC_D2CFGR register.

3.34.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (Edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

3.34.2 General-purpose timers (TIMx)

There are 10 synchronizable general-purpose timers embedded in the STM32H733xG devices (see *Table 4: Timer feature comparison* for differences).

- **TIM2, TIM3, TIM4, TIM5, TIM23, TIM24**

  The devices include four full-featured general-purpose timers: TIM2, TIM3, TIM4, TIM5, TIM23 and TIM24. TIM2, TIM5, TIM23 and TIM24 are based on a 32-bit autoreload up/downcounter and a 16-bit prescaler while TIM3 and TIM4 are based on a 16-bit autoreload up/downcounter and a 16-bit prescaler. All timers feature 4 independent channels for input capture/output compare, PWM or One-pulse mode output. This gives up to 24 input capture/output compare/PWMs on the largest packages.

  TIM2, TIM3, TIM4, TIM5, TIM23 and TIM24 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5, TIM23, and TIM24 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from one to four hall-effect sensors.

- **TIM12, TIM13, TIM14, TIM15, TIM16, TIM17**

  These timers are based on a 16-bit autoreload upcounter and a 16-bit prescaler. TIM13, TIM14, TIM16 and TIM17 feature one independent channel, whereas TIM12 and TIM15 have two independent channels for input capture/output compare, PWM or One-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5, TIM23, and TIM24 full-featured general-purpose timers or used as simple time bases.

3.34.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

3.34.4 Low-power timers (LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5)

The low-power timers have an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wake up the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / One-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
- Internal clock source: LSE, LSI, HSI or APB clock
- External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

3.34.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

A window option allows the device to be reset when a reload operation is made too early after the previous reload.

3.34.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in Debug mode.

3.34.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.35 Real-time clock (RTC), backup SRAM and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- 17-bit autoreload wake-up timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the V_{BAT} pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when VDD power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in V_{BAT} mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in V_{BAT} mode, but is functional in all low-power modes.

All RTC events (Alarm, wake-up timer, timestamp or tamper) can generate an interrupt and wake up the device from the low-power modes.

3.36 Inter-integrated circuit interface (I2C)

STM32H733xG devices embed five I^2C interfaces.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Wake up from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

3.37 Universal synchronous/asynchronous receiver transmitter (USART)

STM32H733xG devices have five embedded universal synchronous receiver transmitters (USART1, USART2, USART3, USART6, and USART10) and five universal asynchronous receiver transmitters (UART4, UART5, UART7, UART8, and UART9). Refer to *Table 5: USART features* for a summary of USARTx and UARTx features.

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN master/slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 17 Mbit/s.

USART1, USART2, USART3, USART6, and USART10 also provide Smartcard mode (ISO 7816 compliant) and SPI-like communication capability.

The USARTs embed a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

All USART have a clock domain independent from the CPU clock, allowing the USARTx to wake up the MCU from Stop mode. The wake-up from Stop mode is programmable and can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled.

All USART interfaces can be served by the DMA controller.

Table 5. USART features

USART modes/features(1)	USART1/2/3/6/10	UART4/5/7/8/9
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode (master/slave)	X	-
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	X
LIN mode	X	X
Dual clock domain and wake-up from low power mode	X	X
Receiver timeout interrupt	X	X
Modbus communication	X	X
Auto baud rate detection	X	X
Driver Enable	X	X
USART data length	7, 8 and 9 bits	
Tx/Rx FIFO	X	X
Tx/Rx FIFO size	16	

1. X = supported.

3.38 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART (LPUART1). The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUARTs embed a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

The LPUART has a clock domain independent from the CPU clock, and can wake up the system from Stop mode. The wake-up from Stop mode are programmable and can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled.

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baud rates.

LPUART interface can be served by the DMA controller.

3.39 Serial peripheral interface (SPI)/inter- integrated sound interfaces (I2S)

The devices feature up to six SPIs (SPI2S1, SPI2S2, SPI2S3, SPI4, SPI5 and SPI2S6) that allow communicating up to 150 Mbits/s in master and slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives eight master mode frequencies and the frame is configurable from 4 to 32 bits for SPI1/I2S1, SPI2/I2S2, SPI3/I2S3, and from 4 to 16 bits for the other peripherals.

All SPI interfaces support NSS pulse mode, TI mode, Hardware CRC calculation, and 16x 8-bit embedded Rx and Tx FIFOs (SPI1/I2S1, SPI2/I2S2, SPI3/I2S3), and 8x 8-bit embedded Rx and Tx FIFOs (SPI4, SPI5, SPI6/I2S6), all with DMA capability.

Four standard I^2S interfaces (multiplexed with SPI1, SPI2, SPI3 and SPI6) are available. They can be operated in master or slave mode, in half-, full-duplex or simplex communication mode, and can be configured to operate as a 16-/32-bit resolution input or output channel (except SPI2S6 which is limited to 16 bits). Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency. All I^2S interfaces support 16x 8-bit embedded Rx and Tx FIFOs with DMA capability.

3.40 Serial audio interfaces (SAI)

The devices embed two SAIs (SAI1, and SAI4) that allow designing many stereo or mono audio protocols such as I2S, LSB or MSB-justified, PCM/DSP, TDM or AC’97. An SPDIF output is available when the audio block is configured as a transmitter. To bring this level of flexibility and reconfigurability, the SAI contains two independent audio subblocks. Each block has it own clock generator and I/O line controller.
Audio sampling frequencies up to 192 kHz are supported.
In addition, up to six microphones per SAI instance can be supported thanks to an embedded PDM interface, with a maximum of 10 microphones due to pinout constraints.
The SAI can work in master or slave configuration. The audio subblocks can be either receiver or transmitter and can work synchronously or asynchronously (with respect to the other one). The SAI can be connected with other SAIs to work synchronously.

3.41 SPDIFRX Receiver Interface (SPDIFRX)

The SPDIFRX peripheral is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multichannel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The main SPDIFRX features are the following:

- Up to four inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports Audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal is available, the SPDIFRX resamples the incoming signal, decode the Manchester stream, recognize frames, subframes and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named spdif_frame_sync, which toggles at the S/PDIF subframe rate that is used to compute the exact sample rate for clock drift algorithms.

3.42 Single wire protocol master interface (SWPMI)

The Single wire protocol master interface (SWPMI) is the master interface corresponding to the Contactless Frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bitrate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling

SWPMI can be served by the DMA controller.

3.43 Management data input/output (MDIO) slaves

The devices embed an MDIO slave interface it includes the following features:

- 32 MDIO Registers addresses, each of which is managed using separate input and output data registers:
  - 32 x 16-bit firmware read/write, MDIO read-only output data registers
  - 32 x 16-bit firmware read-only, MDIO write-only input data registers
- Configurable slave (port) address
- Independently maskable interrupts/events:
  - MDIO Register write
  - MDIO Register read
  - MDIO protocol error
- Able to operate in and wake up from Stop mode

3.44 SD/SDIO/MMC card host interfaces (SDMMC)

Two SDMMC host interfaces are available. They support *MultiMediaCard System Specification Version 4.51* in three different databus modes: 1 bit (default), 4 bits and 8 bits.

Both interfaces support the *SD memory card specifications version 4.1.* and the *SDIO card specification version 4.0.* in two different databus modes: 1 bit (default) and 4 bits.

Each SDMMC host interface supports only one SD/SDIO/MMC card at any one time and a stack of MMC Version 4.51 or previous.

The SDMMC host interface embeds a dedicated DMA controller allowing high-speed transfers between the interface and the SRAM.

3.45 Controller area network (FDCAN1, FDCAN2, FDCAN3)

The controller area network (CAN) subsystem consists of two CAN modules, a shared message RAM memory and a clock calibration unit.

All CAN modules (FDCAN1, FDCAN2, and FDCAN3) are compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

FDCAN1 supports time triggered CAN (TT-FDCAN) specified in ISO 11898-4, including event synchronized time-triggered communication, global system time, and clock drift compensation. The FDCAN1 contains additional registers, specific to the time triggered feature. The CAN FD option can be used together with event-triggered and time-triggered CAN communication.

A 10-Kbyte message RAM memory implements filters, receive FIFOs, receive buffers, transmit event FIFOs, transmit buffers (and triggers for TT-FDCAN). This message RAM is shared between the three modules - FDCAN1 FDCAN2 and FDCAN3.

The common clock calibration unit is optional. It can be used to generate a calibrated clock for FDCAN1, FDCAN2 and FDCAN3 from the HSI internal RC oscillator and the PLL, by evaluating CAN messages received by the FDCAN1.

3.46 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed a USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral that supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 Mbit/s) and a UTMI low-pin interface (ULPI) for high-speed operation (480 Mbit/s). When using the USB OTG_HS interface in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG_HS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It features software-configurable endpoint setting and supports suspend/resume. The USB OTG_HS controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The main features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.47 Ethernet MAC interface with dedicated DMA controller (ETH)

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

3.48 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The devices embed a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wake up the MCU from Stop mode on data reception.

3.49 Debug infrastructure

The devices offer a comprehensive set of debug and trace features to support software development and system integration.

- Breakpoint debugging
- Code execution tracing
- Software instrumentation
- JTAG debug port
- Serial-wire debug port
- Trigger input and output
- Serial-wire trace port
- Trace port
- Arm® CoreSight™ debug and trace components

The debug can be controlled via a JTAG/Serial-wire debug access port, using industry-standard debugging tools. The trace port performs data capture for logging and analysis.

4 Memory mapping

Refer to the product line reference manual for details on the memory mapping as well as the boundary addresses for all peripherals.

5 Pinouts, pin descriptions and alternate functions

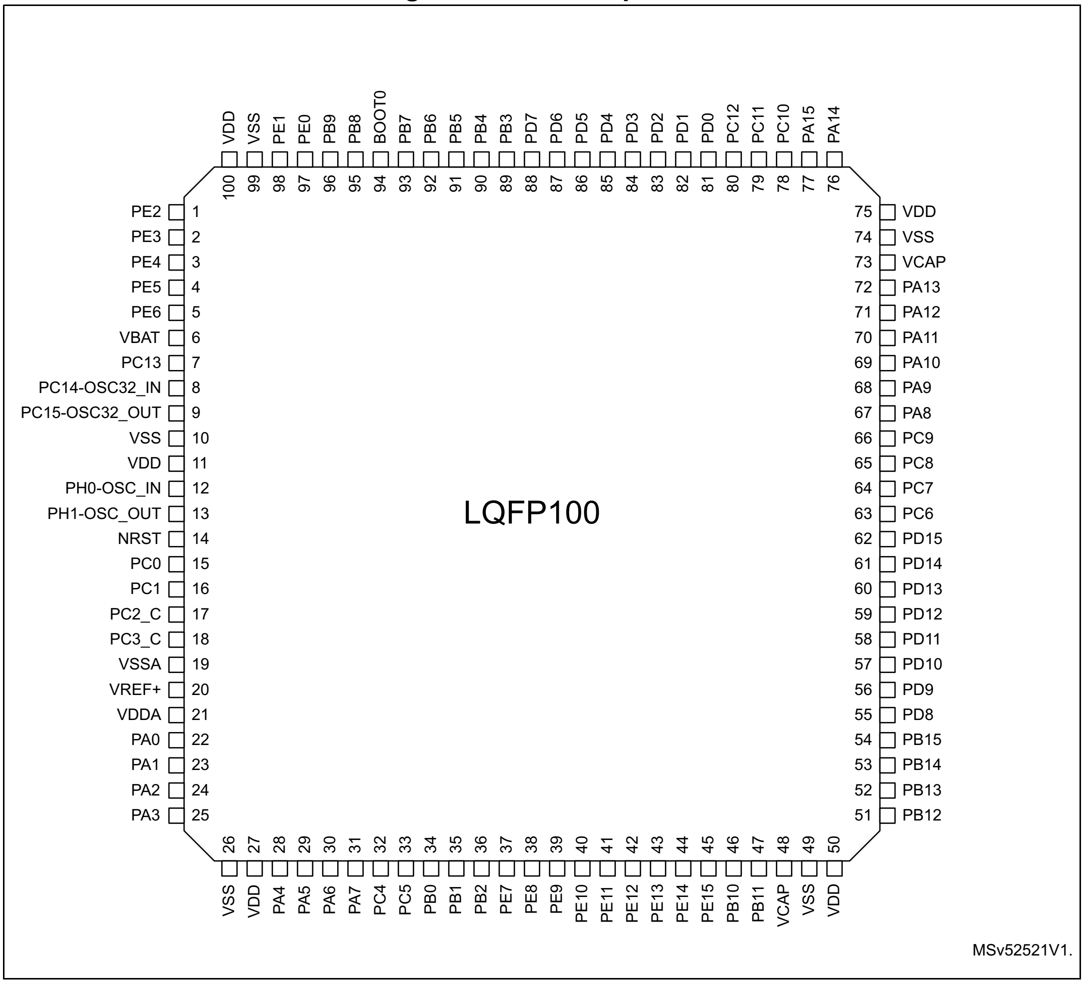
Figure 4. TFBGA100 pinout

	1	2	3	4	5	6	7	8	9	10
A	PC14-OSC32_IN	PC13	PE2	PB9	PB7	PB4	PB3	PA15	PA14	PA13
B	PC15-OSC32_OUT	VBAT	PE3	PB8	PB6	PD5	PD2	PC11	PC10	PA12
C	PH0-OSC_IN	VSS	PE4	PE1	PB5	PD6	PD3	PC12	PA9	PA11
D	PH1-OSC_OUT	VDD	PE5	PE0	BOOT0	PD7	PD4	PD0	PA8	PA10
E	NRST	PC2_C	PE6	VSS	VSS	VSS	VCAP	PD1	PC9	PC7
F	PC0	PC1	PC3_C	VDD	VDD	VDD33USB	PDR_ON	VCAP	PC8	PC6
G	VSSA	PA0	PA4	PC4	PB2	PE10	PE14	PD15	PD11	PB15
H	VDDA	PA1	PA5	PC5	PE7	PE11	PE15	PD14	PD10	PB14
J	VSS	PA2	PA6	PB0	PE8	PE12	PB10	PB13	PD9	PD13
K	VDD	PA3	PA7	PB1	PE9	PE13	PB11	PB12	PD8	PD12

MSv52520V1.

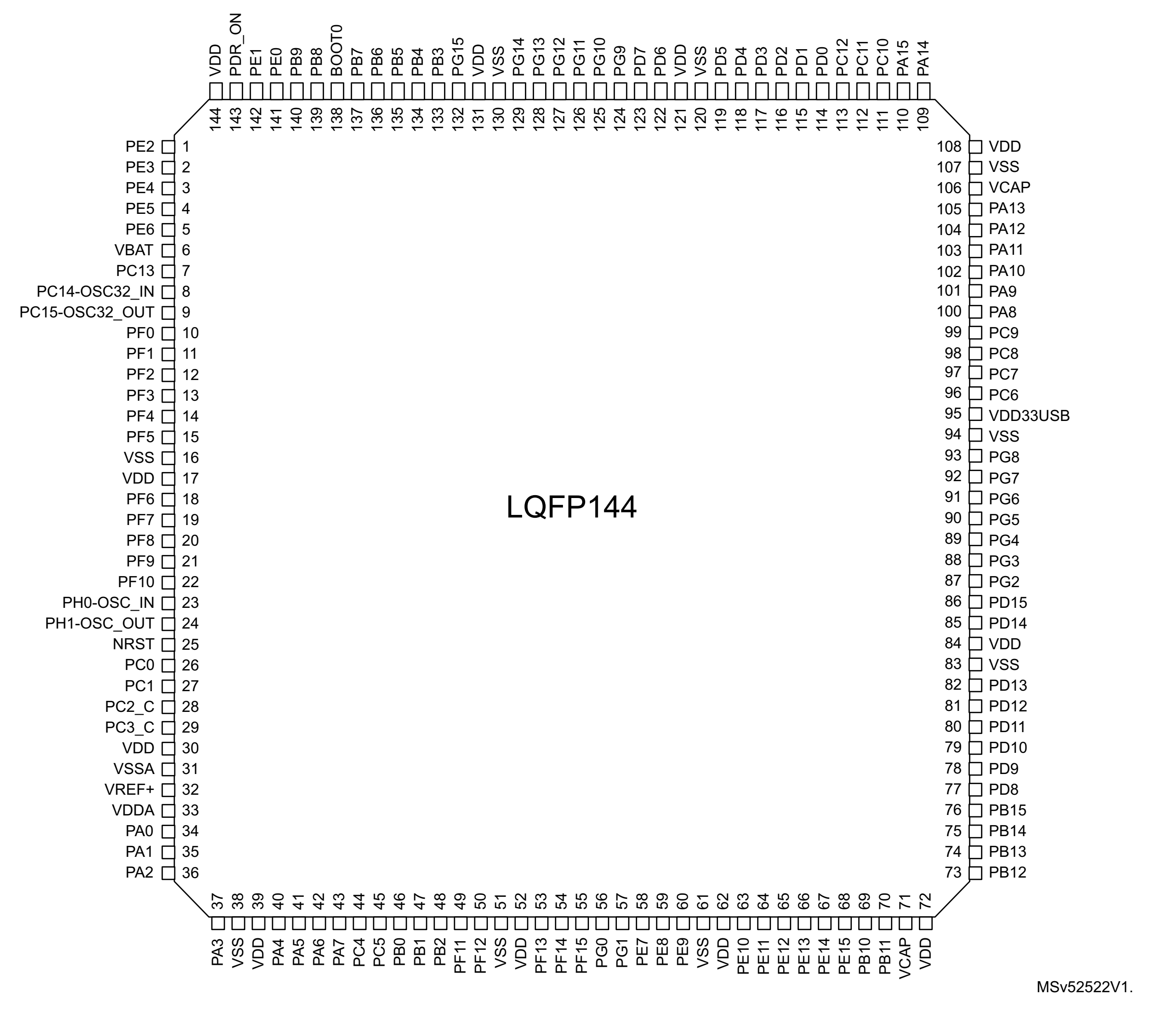
1. The above figure shows the package top view.

Figure 5. LQFP100 pinout



1. The above figure shows the package top view.

Figure 6. LQFP144 pinout



1. The above figure shows the package top view.

Figure 7. UFBGA144 ballout

	1	2	3	4	5	6	7	8	9	10	11	12
A	PC13	PE3	PE2	PE1	PE0	PB4	PB3	PD6	PD7	PA15	PA14	PA13
B	PC14-OSC32_IN	PE4	PE5	PE6	PB9	PB5	PG15	PG12	PD5	PC11	PC10	PA12
C	PC15-OSC32_OUT	VBAT	PF0	PF1	PB8	PB6	PG14	PG11	PD4	PC12	VDD33USB	PA11
D	PH0-OSC_IN	VSS	VDD	PF2	BOOT0	PB7	PG13	PG10	PD3	PD1	PA10	PA9
E	PH1-OSC_OUT	PF3	PF4	PF5	PDR_ON	VSS	VSS	PG9	PD2	PD0	PC9	PA8
F	NRST	PF7	PF6	VDD	VDD	VDD	VDD	VDD	VDD	VDD	PC8	PC7
G	PF10	PF9	PF8	VSS	VDD	VDD	VDD	VSS	VCAP	VSS	PG8	PC6
H	PC0	PC1	PC2	PC3	VSS	VSS	VCAP	PE11	PD11	PG7	PG6	PG5
J	VSSA	PA0	PA4	PC4	PB2	PG1	PE10	PE12	PD10	PG4	PG3	PG2
K	VREF-	PA1	PA5	PC5	PF13	PG0	PE9	PE13	PD9	PD13	PD14	PD15
L	VREF+	PA2	PA6	PB0	PF12	PF15	PE8	PE14	PD8	PD12	PB14	PB15
M	VDDA	PA3	PA7	PB1	PF11	PF14	PE7	PE15	PB10	PB11	PB12	PB13

MSv52523V1.

1. The above figure shows the package top view.

Table 6. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
	ANA	Analog-only Input
I/O structure	FT	5 V tolerant I/O
	TT	3.3 V tolerant I/O
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor
	Option for TT and FT I/Os	
	_f	I2C FM+ option
	_a	analog option (supplied by V_{DDA})
	_u	USB option (supplied by $V_{DD33USB}$)
	_h	High-speed low-voltage I/O
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	

Table 6. Legend/abbreviations used in the pinout table (continued)

Name	Abbreviation	Definition
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers
	Additional functions	Functions directly selected/enabled through peripheral registers

Table 7. STM32H733 pin and ball descriptions

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100	LQFP100	LQFP144	UFBGA144						
A3	1	1	A3	PE2	I/O	FT_h	-	TRACECLK, SAI1_CK1, USART10_RX, SPI4_SCK, SAI1_MCLK_A, SAI4_MCLK_A, OCTOSPIM_P1_IO2, SAI4_CK1, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
B3	2	2	A2	PE3	I/O	FT_h	-	TRACED0, TIM15_BKIN, SAI1_SD_B, SAI4_SD_B, USART10_TX, FMC_A19, EVENTOUT	-
C3	3	3	B2	PE4	I/O	FT_h	-	TRACED1, SAI1_D2, DFSDM1_DATIN3, TIM15_CH1N, SPI4_NSS, SAI1_FS_A, SAI4_FS_A, SAI4_D2, FMC_A20, DCMI_D4/PSSI_D4, LCD_B0, EVENTOUT	-
D3	4	4	B3	PE5	I/O	FT_h	-	TRACED2, SAI1_CK2, DFSDM1_CKIN3, TIM15_CH1, SPI4_MISO, SAI1_SCK_A, SAI4_SCK_A, SAI4_CK2, FMC_A21, DCMI_D6/PSSI_D6, LCD_G0, EVENTOUT	-
E3	5	5	B4	PE6	I/O	FT_h	-	TRACED3, TIM1_BKIN2, SAI1_D1, TIM15_CH2, SPI4_MOSI, SAI1_SD_A, SAI4_SD_A, SAI4_D1, SAI4_MCLK_B, TIM1_BKIN2_COMP12, FMC_A22, DCMI_D7/PSSI_D7, LCD_G1, EVENTOUT	-
B2	6	6	C2	VBAT	S	-	-	-	-
A2	7	7	A1	PC13	I/O	FT	-	EVENTOUT	RTC_TAMP1/ RTC_TS, WKUP4
A1	8	8	B1	PC14-OSC32_IN	I/O	FT	-	EVENTOUT	OSC32_IN
B1	9	9	C1	PC15-OSC32_OUT	I/O	FT	-	EVENTOUT	OSC32_OUT

Table 7. STM32H733 pin and ball descriptions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100	LQFP100	LQFP144	UFBGA144						
-	-	10	C3	PF0	I/O	FT_fh	-	I2C2_SDA(boot), I2C5_SDA, OCTOSPIM_P2_IO0, FMC_A0, TIM23_CH1, EVENTOUT	-
-	-	11	C4	PF1	I/O	FT_fh	-	I2C2_SCL(boot), I2C5_SCL, OCTOSPIM_P2_IO1, FMC_A1, TIM23_CH2, EVENTOUT	-
-	-	12	D4	PF2	I/O	FT_h	-	I2C2_SMBA, I2C5_SMBA, OCTOSPIM_P2_IO2, FMC_A2, TIM23_CH3, EVENTOUT	-
-	-	13	E2	PF3	I/O	FT_ha	-	OCTOSPIM_P2_IO3, FMC_A3, TIM23_CH4, EVENTOUT	ADC3_INP5
-	-	14	E3	PF4	I/O	FT_ha	-	OCTOSPIM_P2_CLK, FMC_A4, EVENTOUT	ADC3_INN5, ADC3_INP9
-	-	15	E4	PF5	I/O	FT_ha	-	OCTOSPIM_P2_NCLK, FMC_A5, EVENTOUT	ADC3_INP4
-	10	16	-	VSS	S	-	-	-	-
-	11	17	-	VDD	S	-	-	-	-
-	-	18	F3	PF6	I/O	FT_ha	-	TIM16_CH1, FDCAN3_RX, SPI5_NSS, SAI1_SD_B, UART7_RX, SAI4_SD_B, OCTOSPIM_P1_IO3, TIM23_CH1, EVENTOUT	ADC3_INN4, ADC3_INP8
-	-	19	F2	PF7	I/O	FT_ha	-	TIM17_CH1, FDCAN3_TX, SPI5_SCK, SAI1_MCLK_B, UART7_TX, SAI4_MCLK_B, OCTOSPIM_P1_IO2, TIM23_CH2, EVENTOUT	ADC3_INP3
-	-	20	G3	PF8	I/O	FT_ha	-	TIM16_CH1N, SPI5_MISO, SAI1_SCK_B, UART7_RTS/UART7_DE, SAI4_SCK_B, TIM13_CH1, OCTOSPIM_P1_IO0, TIM23_CH3, EVENTOUT	ADC3_INN3, ADC3_INP7
-	-	21	G2	PF9	I/O	FT_ha	-	TIM17_CH1N, SPI5_MOSI, SAI1_FS_B, UART7_CTS, SAI4_FS_B, TIM14_CH1, OCTOSPIM_P1_IO1, TIM23_CH4, EVENTOUT	ADC3_INP2
-	-	22	G1	PF10	I/O	FT_ha	-	TIM16_BKIN, SAI1_D3, PSSI_D15, OCTOSPIM_P1_CLK, SAI4_D3, DCMI_D11/PSSI_D11, LCD_DE, EVENTOUT	ADC3_INN2, ADC3_INP6
C1	12	23	D1	PH0-OSC_IN	I/O	FT	-	EVENTOUT	OSC_IN

Table 7. STM32H733 pin and ball descriptions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100	LQFP100	LQFP144	UFBGA144						
D1	13	24	E1	PH1-OSC_OUT	I/O	FT	-	EVENTOUT	OSC_OUT
E1	14	25	F1	NRST	I/O	RST	-	-	-
F1	15	26	H1	PC0	I/O	FT_ha	-	FMC_D12/FMC_AD12, DFSDM1_CKIN0, DFSDM1_DATIN4, SAI4_FS_B, FMC_A25, OTG_HS_ULPI_STP, LCD_G2, FMC_SDNWE, LCD_R5, EVENTOUT	ADC123_INP10
F2	16	27	H2	PC1	I/O	FT_ha	-	TRACED0, SAI4_D1, SAI1_D1, DFSDM1_DATIN0, DFSDM1_CKIN4, SPI2_MOSI/I2S2_SDO, SAI1_SD_A, SAI4_SD_A, SDMMC2_CK, OCTOSPIM_P1_IO4, ETH_MDC, MDIOS_MDC, LCD_G5, EVENTOUT	ADC123_INN10, ADC123_INP11, RTC_TAMP3, WKUP6
-	-	-	H3	PC2	I/O	FT_a	-	PWR_DEEPSLEEP, DFSDM1_CKIN1, OCTOSPIM_P1_IO5, SPI2_MISO/I2S2_SDI, DFSDM1_CKOUT, OCTOSPIM_P1_IO2, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT	ADC123_INN11, ADC123_INP12
E2 (1)	17 (1)	28 (1)	-	PC2_C(2)	ANA	TT_a	-	-	ADC3_INN1, ADC3_INP0
-	-	-	H4	PC3	I/O	FT_a	-	PWR_SLEEP, DFSDM1_DATIN1, OCTOSPIM_P1_IO6, SPI2_MOSI/I2S2_SDO, OCTOSPIM_P1_IO0, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT	ADC12_INN12, ADC12_INP13
F3 (1)	18 (1)	29 (1)	-	PC3_C(2)	ANA	TT_a	-	-	ADC3_INP1
-	-	30	-	VDD	S	-	-	-	-
G1	19	31	J1	VSSA	S	-	-	-	-
-	-	-	K1	VREF-	S	-	-	-	-
-	20	32	L1	VREF+	S	-	-	-	-
H1	21	33	M1	VDDA	S	-	-	-	-

Table 7. STM32H733 pin and ball descriptions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100	LQFP100	LQFP144	UFBGA144						
G2	22	34	J2	PA0	I/O	FT_ha	-	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, TIM15_BKIN, SPI6_NSS/I2S6_WS, USART2_CTS/USART2_NSS, UART4_TX, SDMMC2_CMD, SAI4_SD_B, ETH_MII_CRS, FMC_A19, EVENTOUT	ADC1_INP16, WKUP1
H2	23	35	K2	PA1	I/O	FT_ha	-	TIM2_CH2, TIM5_CH2, LPTIM3_OUT, TIM15_CH1N, USART2_RTS/USART2_DE, UART4_RX, OCTOSPIM_P1_IO3, SAI4_MCLK_B, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, OCTOSPIM_P1_DQS, LCD_R2, EVENTOUT	ADC1_INN16, ADC1_INP17
J2	24	36	L2	PA2	I/O	FT_ha	-	TIM2_CH3, TIM5_CH3, LPTIM4_OUT, TIM15_CH1, OCTOSPIM_P1_IO0, USART2_TX(boot), SAI4_SCK_B, ETH_MDIO, MDIOS_MDIO, LCD_R1, EVENTOUT	ADC12_INP14, WKUP2
K2	25	37	M2	PA3	I/O	FT_ha	-	TIM2_CH4, TIM5_CH4, LPTIM5_OUT, TIM15_CH2, I2S6_MCK, OCTOSPIM_P1_IO2, USART2_RX(boot), LCD_B2, OTG_HS_ULPI_D0, ETH_MII_COL, OCTOSPIM_P1_CLK, LCD_B5, EVENTOUT	ADC12_INP15
-	26	38	-	VSS	S	-	-	-	-
-	27	39	-	VDD	S	-	-	-	-
G3	28	40	J3	PA4	I/O	TT_ha	-	D1PWREN, TIM5_ETR, SPI1_NSS(boot)/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS/I2S6_WS, FMC_D8/FMC_AD8, DCMI_HSYNC/PSSI_DE, LCD_VSYNC, EVENTOUT	ADC12_INP18, DAC1_OUT1
H3	29	41	K3	PA5	I/O	TT_ha	-	D2PWREN, TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK(boot)/I2S1_CK, SPI6_SCK/I2S6_CK, OTG_HS_ULPI_CK, FMC_D9/FMC_AD9, PSSI_D14, LCD_R4, EVENTOUT	ADC12_INN18, ADC12_INP19, DAC1_OUT2

Table 7. STM32H733 pin and ball descriptions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100	LQFP100	LQFP144	UFBGA144						
J3	30	42	L3	PA6	I/O	FT_ha	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO(boot)/I2S1_SDI, OCTOSPIM_P1_IO3, SPI6_MISO/I2S6_SDI, TIM13_CH1, TIM8_BKIN_COMP12, MDIOS_MDC, TIM1_BKIN_COMP12, DCMI_PIXCLK/PSSI_PDCK, LCD_G2, EVENTOUT	ADC12_INP3
K3	31	43	M3	PA7	I/O	TT_ha	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI(boot)/I2S1_SDO, SPI6_MOSI/I2S6_SDO, TIM14_CH1, OCTOSPIM_P1_IO2, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, LCD_VSYNC, EVENTOUT	ADC12_INN3, ADC12_INP7, OPAMP1_VINM
G4	32	44	J4	PC4	I/O	TT_ha	-	PWR_DEEPSLEEP, FMC_A22, DFSDM1_CKIN2, I2S1_MCK, SPDIFRX1_IN3, SDMMC2_CKIN, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, LCD_R7, EVENTOUT	ADC12_INP4, OPAMP1_VOUT, COMP1_INM
H4	33	45	K4	PC5	I/O	TT_ha	-	PWR_SLEEP, SAI4_D3, SAI1_D3, DFSDM1_DATIN2, PSSI_D15, SPDIFRX1_IN4, OCTOSPIM_P1_DQS, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, COMP1_OUT, LCD_DE, EVENTOUT	ADC12_INN4, ADC12_INP8, OPAMP1_VINM
J4	34	46	L4	PB0	I/O	TT_ha	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, OCTOSPIM_P1_IO1, DFSDM1_CKOUT, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, LCD_G1, EVENTOUT	ADC12_INN5, ADC12_INP9, OPAMP1_VINP, COMP1_INP
K4	35	47	M4	PB1	I/O	FT_ha	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, OCTOSPIM_P1_IO0, DFSDM1_DATIN1, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, LCD_G0, EVENTOUT	ADC12_INP5, COMP1_INM
G5	36	48	J5	PB2	I/O	FT_ha	-	RTC_OUT, SAI4_D1, SAI1_D1, DFSDM1_CKIN1, SAI1_SD_A, SPI3_MOSI/I2S3_SDO, SAI4_SD_A, OCTOSPIM_P1_CLK, OCTOSPIM_P1_DQS, ETH_TX_ER, TIM23_ETR, EVENTOUT	COMP1_INP

Table 7. STM32H733 pin and ball descriptions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100	LQFP100	LQFP144	UFBGA144						
-	-	49	M5	PF11	I/O	FT_ha	-	SPI5_MOSI, OCTOSPIM_P1_NCLK, SAI4_SD_B, FMC_NRAS, DCMI_D12/PSSI_D12, TIM24_CH1, EVENTOUT	ADC1_INP2
-	-	50	L5	PF12	I/O	FT_ha	-	OCTOSPIM_P2_DQS, FMC_A6, TIM24_CH2, EVENTOUT	ADC1_INN2, ADC1_INP6
-	-	51	-	VSS	S	-	-	-	-
-	-	52	-	VDD	S	-	-	-	-
-	-	53	K5	PF13	I/O	FT_ha	-	DFSDM1_DATIN6, I2C4_SMBA, FMC_A7, TIM24_CH3, EVENTOUT	ADC2_INP2
-	-	54	M6	PF14	I/O	FT_fha	-	DFSDM1_CKIN6, I2C4_SCL, FMC_A8, TIM24_CH4, EVENTOUT	ADC2_INN2, ADC2_INP6
-	-	55	L6	PF15	I/O	FT_fh	-	I2C4_SDA, FMC_A9, EVENTOUT	-
-	-	56	K6	PG0	I/O	FT_h	-	OCTOSPIM_P2_IO4, UART9_RX, FMC_A10, EVENTOUT	-
-	-	57	J6	PG1	I/O	TT_h	-	OCTOSPIM_P2_IO5, UART9_TX, FMC_A11, EVENTOUT	OPAMP2_VINM
H5	37	58	M7	PE7	I/O	TT_ha	-	TIM1_ETR, DFSDM1_DATIN2, UART7_RX, OCTOSPIM_P1_IO4, FMC_D4/FMC_AD4, EVENTOUT	OPAMP2_VOUT, COMP2_INM
J5	38	59	L7	PE8	I/O	TT_ha	-	TIM1_CH1N, DFSDM1_CKIN2, UART7_TX, OCTOSPIM_P1_IO5, FMC_D5/FMC_AD5, COMP2_OUT, EVENTOUT	OPAMP2_VINM
K5	39	60	K7	PE9	I/O	TT_ha	-	TIM1_CH1, DFSDM1_CKOUT, UART7_RTS/UART7_DE, OCTOSPIM_P1_IO6, FMC_D6/FMC_AD6, EVENTOUT	OPAMP2_VINP, COMP2_INP
-	-	61	-	VSS	S	-	-	-	-
-	-	62	-	VDD	S	-	-	-	-
G6	40	63	J7	PE10	I/O	FT_ha	-	TIM1_CH2N, DFSDM1_DATIN4, UART7_CTS, OCTOSPIM_P1_IO7, FMC_D7/FMC_AD7, EVENTOUT	COMP2_INM
H6	41	64	H8	PE11	I/O	FT_ha	-	TIM1_CH2, DFSDM1_CKIN4, SPI4_NSS(boot), SAI4_SD_B, OCTOSPIM_P1_NCS, FMC_D8/FMC_AD8, LCD_G3, EVENTOUT	COMP2_INP

Table 7. STM32H733 pin and ball descriptions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100	LQFP100	LQFP144	UFBGA144						
J6	42	65	J8	PE12	I/O	FT_h	-	TIM1_CH3N, DFSDM1_DATIN5, SPI4_SCK(boot), SAI4_SCK_B, FMC_D9/FMC_AD9, COMP1_OUT, LCD_B4, EVENTOUT	-
K6	43	66	K8	PE13	I/O	FT_h	-	TIM1_CH3, DFSDM1_CKIN5, SPI4_MISO(boot), SAI4_FS_B, FMC_D10/FMC_AD10, COMP2_OUT, LCD_DE, EVENTOUT	-
G7	44	67	L8	PE14	I/O	FT_h	-	TIM1_CH4, SPI4_MOSI(boot), SAI4_MCLK_B, FMC_D11/FMC_AD11, LCD_CLK, EVENTOUT	-
H7	45	68	M8	PE15	I/O	FT_h	-	TIM1_BKIN, USART10_CK, FMC_D12/FMC_AD12, TIM1_BKIN_COMP12, LCD_R7, EVENTOUT	-
J7	46	69	M9	PB10	I/O	FT_fh	-	TIM2_CH3, LPTIM2_IN1, I2C2_SCL, SPI2_SCK/I2S2_CK, DFSDM1_DATIN7, USART3_TX(boot), OCTOSPIM_P1_NCS, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	-
K7	47	70	M10	PB11	I/O	FT_f	-	TIM2_CH4, LPTIM2_ETR, I2C2_SDA, DFSDM1_CKIN7, USART3_RX(boot), OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, LCD_G5, EVENTOUT	-
F8	48	71	H7	VCAP	S	-	-	-	-
-	49	-	-	VSS	S	-	-	-	-
-	50	72	-	VDD	S	-	-	-	-
K8	51	73	M11	PB12	I/O	FT_h	-	TIM1_BKIN, OCTOSPIM_P1_NCLK, I2C2_SMBA, SPI2_NSS/I2S2_WS, DFSDM1_DATIN1, USART3_CK, FDCAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OCTOSPIM_P1_IO0, TIM1_BKIN_COMP12, UART5_RX, EVENTOUT	-

Table 7. STM32H733 pin and ball descriptions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100	LQFP100	LQFP144	UFBGA144						
J8	52	74	M12	PB13	I/O	FT_h	-	TIM1_CH1N, LPTIM2_OUT, OCTOSPIM_P1_IO2, SPI2_SCK/I2S2_CK, DFSDM1_CKIN1, USART3_CTS/USART3_NSS, FDCAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, SDMMC1_D0, DCMI_D2/PSSI_D2, UART5_TX, EVENTOUT	-
H10	53	75	L11	PB14	I/O	FT_h	-	TIM1_CH2N, TIM12_CH1, TIM8_CH2N, USART1_TX, SPI2_MISO/I2S2_SDI, DFSDM1_DATIN2, USART3_RTS/USART3_DE, UART4_RTS/UART4_DE, SDMMC2_D0, FMC_D10/FMC_AD10, LCD_CLK, EVENTOUT	-
G10	54	76	L12	PB15	I/O	FT_h	-	RTC_REFIN, TIM1_CH3N, TIM12_CH2, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SDO, DFSDM1_CKIN2, UART4_CTS, SDMMC2_D1, FMC_D11/FMC_AD11, LCD_G7, EVENTOUT	-
K9	55	77	L9	PD8	I/O	FT_h	-	DFSDM1_CKIN3, USART3_TX(boot), SPDIFRX1_IN2, FMC_D13/FMC_AD13, EVENTOUT	-
J9	56	78	K9	PD9	I/O	FT_h	-	DFSDM1_DATIN3, USART3_RX(boot), FMC_D14/FMC_AD14, EVENTOUT	-
H9	57	79	J9	PD10	I/O	FT_h	-	DFSDM1_CKOUT, USART3_CK, FMC_D15/FMC_AD15, LCD_B3, EVENTOUT	-
G9	58	80	H9	PD11	I/O	FT_h	-	LPTIM2_IN2, I2C4_SMBA, USART3_CTS/USART3_NSS, OCTOSPIM_P1_IO0, SAI4_SD_A, FMC_A16/FMC_CLE, EVENTOUT	-
K10	59	81	L10	PD12	I/O	FT_fh	-	LPTIM1_IN1, TIM4_CH1, LPTIM2_IN1, I2C4_SCL, FDCAN3_RX, USART3_RTS/USART3_DE, OCTOSPIM_P1_IO1, SAI4_FS_A, FMC_A17/FMC_ALE, DCMI_D12/PSSI_D12, EVENTOUT	-

Table 7. STM32H733 pin and ball descriptions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100	LQFP100	LQFP144	UFBGA144						
J10	60	82	K10	PD13	I/O	FT_fh	-	LPTIM1_OUT, TIM4_CH2, I2C4_SDA, FDCAN3_TX, OCTOSPIM_P1_IO3, SAI4_SCK_A, UART9_RTS/UART9_DE, FMC_A18, DCMI_D13/PSSI_D13, EVENTOUT	-
-	-	83	-	VSS	S	-	-	-	-
-	-	84	-	VDD	S	-	-	-	-
H8	61	85	K11	PD14	I/O	FT_h	-	TIM4_CH3, UART8_CTS, UART9_RX, FMC_D0/FMC_AD0, EVENTOUT	-
G8	62	86	K12	PD15	I/O	FT_h	-	TIM4_CH4, UART8_RTS/UART8_DE, UART9_TX, FMC_D1/FMC_AD1, EVENTOUT	-
-	-	87	J12	PG2	I/O	FT_h	-	TIM8_BKIN, TIM8_BKIN_COMP12, FMC_A12, TIM24_ETR, EVENTOUT	-
-	-	88	J11	PG3	I/O	FT_h	-	TIM8_BKIN2, TIM8_BKIN2_COMP12, FMC_A13, TIM23_ETR, EVENTOUT	-
-	-	89	J10	PG4	I/O	FT_h	-	TIM1_BKIN2, TIM1_BKIN2_COMP12, FMC_A14/FMC_BA0, EVENTOUT	-
-	-	90	H12	PG5	I/O	FT_h	-	TIM1_ETR, FMC_A15/FMC_BA1, EVENTOUT	-
-	-	91	H11	PG6	I/O	FT_h	-	TIM17_BKIN, OCTOSPIM_P1_NCS, FMC_NE3, DCMI_D12/PSSI_D12, LCD_R7, EVENTOUT	-
-	-	92	H10	PG7	I/O	FT_h	-	SAI1_MCLK_A, USART6_CK, OCTOSPIM_P2_DQS, FMC_INT, DCMI_D13/PSSI_D13, LCD_CLK, EVENTOUT	-
-	-	93	G11	PG8	I/O	FT_h	-	TIM8_ETR, SPI6_NSS/I2S6_WS, USART6_RTS/USART6_DE, SPDIFRX1_IN3, ETH_PPS_OUT, FMC_SDCLK, LCD_G7, EVENTOUT	-
-	-	94	-	VSS	S	-	-	-	-
F6	-	95	C11	VDD33USB	S	-	-	-	-
F10	63	96	G12	PC6	I/O	FT_h	-	TIM3_CH1, TIM8_CH1, DFSDM1_CKIN3, I2S2_MCK, USART6_TX, SDMMC1_D0DIR, FMC_NWAIT, SDMMC2_D6, SDMMC1_D6, DCMI_D0/PSSI_D0, LCD_HSYNC, EVENTOUT	SWPMI_IO

Table 7. STM32H733 pin and ball descriptions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100	LQFP100	LQFP144	UFBGA144						
E10	64	97	F12	PC7	I/O	FT_h	-	DBTRGIO, TIM3_CH2, TIM8_CH2, DFSDM1_DATIN3, I2S3_MCK, USART6_RX, SDMMC1_D123DIR, FMC_NE1, SDMMC2_D7, SWPMI_TX, SDMMC1_D7, DCMI_D1/PSSI_D1, LCD_G6, EVENTOUT	-
F9	65	98	F11	PC8	I/O	FT_h	-	TRACED1, TIM3_CH3, TIM8_CH3, USART6_CK, UART5_RTS/UART5_DE, FMC_NE2/FMC_NCE, FMC_INT, SWPMI_RX, SDMMC1_D0, DCMI_D2/PSSI_D2, EVENTOUT	-
E9	66	99	E11	PC9	I/O	FT_fh	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA(boot), I2S_CKIN, I2C5_SDA, UART5_CTS, OCTOSPIM_P1_IO0, LCD_G3, SWPMI_SUSPEND, SDMMC1_D1, DCMI_D3/PSSI_D3, LCD_B2, EVENTOUT	-
D9	67	100	E12	PA8	I/O	FT_fh	-	MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL(boot), I2C5_SCL, USART1_CK, OTG_HS_SOF, UART7_RX, TIM8_BKIN2_COMP12, LCD_B3, LCD_R6, EVENTOUT	-
C9	68	101	D12	PA9	I/O	FT_u	-	TIM1_CH2, LPUART1_TX, I2C3_SMBA, SPI2_SCK/I2S2_CK, I2C5_SMBA, USART1_TX(boot), ETH_TX_ER, DCMI_D0/PSSI_D0, LCD_R5, EVENTOUT	OTG_HS_VBUS
D10	69	102	D11	PA10	I/O	FT_u	-	TIM1_CH3, LPUART1_RX, USART1_RX(boot), OTG_HS_ID, MDIOS_MDIO, LCD_B4, DCMI_D1/PSSI_D1, LCD_B1, EVENTOUT	-
C10	70	103	C12	PA11	I/O	FT_u	-	TIM1_CH4, LPUART1_CTS, SPI2_NSS/I2S2_WS, UART4_RX, USART1_CTS/USART1_NSS, FDCAN1_RX, LCD_R4, EVENTOUT	OTG_HS_DM (boot)
B10	71	104	B12	PA12	I/O	FT_u	-	TIM1_ETR, LPUART1_RTS/LPUART1_DE, SPI2_SCK/I2S2_CK, UART4_TX, USART1_RTS/USART1_DE, SAI4_FS_B, FDCAN1_TX, TIM1_BKIN2, LCD_R5, EVENTOUT	OTG_HS_DP (boot)

Table 7. STM32H733 pin and ball descriptions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100	LQFP100	LQFP144	UFBGA144						
A10	72	105	A12	PA13(JTMS/SWDIO)	I/O	FT	-	JTMS/SWDIO, EVENTOUT	-
E7	73	106	G9	VCAP	S	-	-	-	-
-	74	107	-	VSS	S	-	-	-	-
-	75	108	-	VDD	S	-	-	-	-
A9	76	109	A11	PA14(JTCK/SWCLK)	I/O	FT	-	JTCK/SWCLK, EVENTOUT	-
A8	77	110	A10	PA15(JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, CEC, SPI1_NSS/I2S1_WS, SPI3_NSS(boot)/I2S3_WS, SPI6_NSS/I2S6_WS, UART4_RTS/UART4_DE, LCD_R3, UART7_TX, LCD_B6, EVENTOUT	-
B9	78	111	B11	PC10	I/O	FT_fh	-	DFSDM1_CKIN5, I2C5_SDA, SPI3_SCK(boot)/I2S3_CK, USART3_TX, UART4_TX, OCTOSPIM_P1_IO1, LCD_B1, SWPMI_RX, SDMMC1_D2, DCMI_D8/PSSI_D8, LCD_R2, EVENTOUT	-
B8	79	112	B10	PC11	I/O	FT_fh	-	DFSDM1_DATIN5, I2C5_SCL, SPI3_MISO(boot)/I2S3_SDI, USART3_RX, UART4_RX, OCTOSPIM_P1_NCS, SDMMC1_D3, DCMI_D4/PSSI_D4, LCD_B4, EVENTOUT	-
C8	80	113	C10	PC12	I/O	FT_h	-	TRACED3, FMC_D6/FMC_AD6, TIM15_CH1, I2C5_SMBA, SPI6_SCK/I2S6_CK, SPI3_MOSI(boot)/I2S3_SDO, USART3_CK, UART5_TX, SDMMC1_CK, DCMI_D9/PSSI_D9, LCD_R6, EVENTOUT	-
D8	81	114	E10	PD0	I/O	FT_h	-	DFSDM1_CKIN6, UART4_RX, FDCAN1_RX(boot), UART9_CTS, FMC_D2/FMC_AD2, LCD_B1, EVENTOUT	-
E8	82	115	D10	PD1	I/O	FT_h	-	DFSDM1_DATIN6, UART4_TX, FDCAN1_TX(boot), FMC_D3/FMC_AD3, EVENTOUT	-

Table 7. STM32H733 pin and ball descriptions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100	LQFP100	LQFP144	UFBGA144						
B7	83	116	E9	PD2	I/O	FT_h	-	TRACED2, FMC_D7/FMC_AD7, TIM3_ETR, TIM15_BKIN, UART5_RX, LCD_B7, SDMMC1_CMD, DCMI_D11/PSSI_D11, LCD_B2, EVENTOUT	-
C7	84	117	D9	PD3	I/O	FT_h	-	DFSDM1_CKOUT, SPI2_SCK/I2S2_CK, USART2_CTS/USART2_NSS, FMC_CLK, DCMI_D5/PSSI_D5, LCD_G7, EVENTOUT	-
D7	85	118	C9	PD4	I/O	FT_h	-	USART2_RTS/USART2_DE, OCTOSPIM_P1_IO4, FMC_NOE, EVENTOUT	-
B6	86	119	B9	PD5	I/O	FT_h	-	USART2_TX, OCTOSPIM_P1_IO5, FMC_NWE, EVENTOUT	-
-	-	120	-	VSS	S	-	-	-	-
-	-	121	-	VDD	S	-	-	-	-
C6	87	122	A8	PD6	I/O	FT_h	-	SAI4_D1, SAI1_D1, DFSDM1_CKIN4, DFSDM1_DATIN1, SPI3_MOSI/I2S3_SDO, SAI1_SD_A, USART2_RX, SAI4_SD_A, OCTOSPIM_P1_IO6, SDMMC2_CK, FMC_NWAIT, DCMI_D10/PSSI_D10, LCD_B2, EVENTOUT	-
D6	88	123	A9	PD7	I/O	FT_h	-	DFSDM1_DATIN4, SPI1_MOSI/I2S1_SDO, DFSDM1_CKIN1, USART2_CK, SPDIFRX1_IN1, OCTOSPIM_P1_IO7, SDMMC2_CMD, FMC_NE1, EVENTOUT	-
-	-	124	E8	PG9	I/O	FT_h	-	FDCAN3_TX, SPI1_MISO/I2S1_SDI, USART6_RX, SPDIFRX1_IN4, OCTOSPIM_P1_IO6, SAI4_FS_B, SDMMC2_D0, FMC_NE2/FMC_NCE, DCMI_VSYNC/PSSI_RDY, EVENTOUT	-
-	-	125	D8	PG10	I/O	FT_h	-	FDCAN3_RX, OCTOSPIM_P2_IO6, SPI1_NSS/I2S1_WS, LCD_G3, SAI4_SD_B, SDMMC2_D1, FMC_NE3, DCMI_D2/PSSI_D2, LCD_B2, EVENTOUT	-

Table 7. STM32H733 pin and ball descriptions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100	LQFP100	LQFP144	UFBGA144						
-	-	126	C8	PG11	I/O	FT_h	-	LPTIM1_IN2, USART10_RX, SPI1_SCK/I2S1_CK, SPDIFRX1_IN1, OCTOSPIM_P2_IO7, SDMMC2_D2, ETH_MII_TX_EN/ETH_RMII_TX_EN, DCMI_D3/PSSI_D3, LCD_B3, EVENTOUT	-
-	-	127	B8	PG12	I/O	FT_h	-	LPTIM1_IN1, OCTOSPIM_P2_NCS, USART10_TX, SPI6_MISO/I2S6_SDI, USART6_RTS/USART6_DE, SPDIFRX1_IN2, LCD_B4, SDMMC2_D3, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_NE4, TIM23_CH1, LCD_B1, EVENTOUT	-
-	-	128	D7	PG13	I/O	FT_h	-	TRACED0, LPTIM1_OUT, USART10_CTS/USART10_NSS, SPI6_SCK/I2S6_CK, USART6_CTS/USART6_NSS, SDMMC2_D6, ETH_MII_TXD0/ETH_RMII_TXD0, FMC_A24, TIM23_CH2, LCD_R0, EVENTOUT	-
-	-	129	C7	PG14	I/O	FT_h	-	TRACED1, LPTIM1_ETR, USART10_RTS/USART10_DE, SPI6_MOSI/I2S6_SDO, USART6_TX, OCTOSPIM_P1_IO7, SDMMC2_D7, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_A25, TIM23_CH3, LCD_B0, EVENTOUT	-
-	-	130	-	VSS	S	-	-	-	-
-	-	131	-	VDD	S	-	-	-	-
-	-	132	B7	PG15	I/O	FT_h	-	USART6_CTS/USART6_NSS, OCTOSPIM_P2_DQS, USART10_CK, FMC_NCAS, DCMI_D13/PSSI_D13, EVENTOUT	-
A7	89	133	A7	PB3 (JTDO/TRACESWO)	I/O	FT_h	-	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, SPI6_SCK/I2S6_CK, SDMMC2_D2, CRS_SYNC, UART7_RX, TIM24_ETR, EVENTOUT	-

Table 7. STM32H733 pin and ball descriptions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100	LQFP100	LQFP144	UFBGA144						
A6	90	134	A6	PB4(NJTRST)	I/O	FT_h	-	NJTRST, TIM16_BKIN, TIM3_CH1, SPI1_MISO/I2S1_SDI, SPI3_MISO/I2S3_SDI, SPI2_NSS/I2S2_WS, SPI6_MISO/I2S6_SDI, SDMMC2_D3, UART7_TX, EVENTOUT	-
C5	91	135	B6	PB5	I/O	FT_h	-	TIM17_BKIN, TIM3_CH2, LCD_B5, I2C1_SMBA, SPI1_MOSI/I2S1_SDO, I2C4_SMBA, SPI3_MOSI/I2S3_SDO, SPI6_MOSI/I2S6_SDO, FDCAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10/PSSI_D10, UART5_RX, EVENTOUT	-
B5	92	136	C6	PB6	I/O	FT_fh	-	TIM16_CH1N, TIM4_CH1, I2C1_SCL(boot), CEC, I2C4_SCL, USART1_TX, LPUART1_TX, FDCAN2_TX, OCTOSPIM_P1_NCS, DFSDM1_DATIN5, FMC_SDNE1, DCMI_D5/PSSI_D5, UART5_TX, EVENTOUT	-
A5	93	137	D6	PB7	I/O	FT_fa	-	TIM17_CH1N, TIM4_CH2, I2C1_SDA, I2C4_SDA, USART1_RX, LPUART1_RX, DFSDM1_CKIN5, FMC_NL, DCMI_VSYNC/PSSI_RDY, EVENTOUT	PVD_IN
D5	94	138	D5	BOOT0	I	B	-	-	VPP
B4	95	139	C5	PB8	I/O	FT_fh	-	TIM16_CH1, TIM4_CH3, DFSDM1_CKIN7, I2C1_SCL, I2C4_SCL, SDMMC1_CKIN, UART4_RX, FDCAN1_RX, SDMMC2_D4, ETH_MII_TXD3, SDMMC1_D4, DCMI_D6/PSSI_D6, LCD_B6, EVENTOUT	-
A4	96	140	B5	PB9	I/O	FT_fh	-	TIM17_CH1, TIM4_CH4, DFSDM1_DATIN7, I2C1_SDA(boot), SPI2_NSS/I2S2_WS, I2C4_SDA, SDMMC1_CDIR, UART4_TX, FDCAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, DCMI_D7/PSSI_D7, LCD_B7, EVENTOUT	-

Table 7. STM32H733 pin and ball descriptions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100	LQFP100	LQFP144	UFBGA144						
D4	97	141	A5	PE0	I/O	FT_h	-	LPTIM1_ETR, TIM4_ETR, LPTIM2_ETR, UART8_RX, SAI4_MCLK_A, FMC_NBL0, DCMI_D2/PSSI_D2, LCD_R0, EVENTOUT	-
C4	98	142	A4	PE1	I/O	FT_h	-	LPTIM1_IN2, UART8_TX, FMC_NBL1, DCMI_D3/PSSI_D3, LCD_R6, EVENTOUT	-
-	99	-	-	VSS	S	-	-	-	-
F7	-	143	E5	PDR_ON	S	-	-	-	-
-	100	144	-	VDD	S	-	-	-	-
C2	-	-	D2	VSS	S	-	-	-	-
E6	-	-	E6	VSS	S	-	-	-	-
J1	-	-	E7	VSS	S	-	-	-	-
E4	-	-	G4	VSS	S	-	-	-	-
E5	-	-	G8	VSS	S	-	-	-	-
-	-	-	G10	VSS	S	-	-	-	-
-	-	-	H5	VSS	S	-	-	-	-
-	-	-	H6	VSS	S	-	-	-	-
D2	-	-	D3	VDD	S	-	-	-	-
F5	-	-	F4	VDD	S	-	-	-	-
K1	-	-	F5	VDD	S	-	-	-	-
F4	-	-	F6	VDD	S	-	-	-	-
-	-	-	F7	VDD	S	-	-	-	-
-	-	-	F8	VDD	S	-	-	-	-
-	-	-	F9	VDD	S	-	-	-	-
-	-	-	F10	VDD	S	-	-	-	-
-	-	-	G5	VDD	S	-	-	-	-
-	-	-	G6	VDD	S	-	-	-	-
-	-	-	G7	VDD	S	-	-	-	-

1. There is a direct path between Pxy_C and Pxy pins/balls, through an analog switch. Pxy alternate functions are available on Pxy_C when the analog switch is closed. The analog switch is configured through a SYSCFG register. Refer to the product reference manual for a detailed description of the switch configuration bits
2. Pxy_C pins have specific electrical limitations described in *Section 6: Electrical characteristics*.

Table 8. STM32H733 pin alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	FMC/LPTIM1/SAI4/TIM16/17/TIM1x/TIM2x	FDCAN3/PDM_SAI1/TIM3/4/5/12/15	DFSDM1/LCD/LPTIM2/3/4/5/LPUART1/OCTOSPIM_P1/2/TIM8	CEC/DCMI/PSSI/DFSDM1/I2C1/2/3/4/5/LPTIM2/OCTOSPIM_P1/TIM15/USART1/10	CEC/FDCAN3/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	DFSDM1/I2C4/5/OCTOSPIM_P1/SAI1/SPI3/I2S3/UART4	SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/UART7/USART1/2/3/6	LPUART1/SAI4/SDMMC1/SPDIFRX1/SPI6/UART4/5/8	FDCAN1/2/FMC/LCD/OCTOSPIM_P1/2/SAI4/SDMMC2/SPDIFRX1/TIM13/14	CRS/FMC/LCD/OCTOSPIM_P1/OTG1_FS/OTG1_HS/SAI4/SDMMC2/TIM8	DFSDM1/ETH/I2C4/LCD/MDIOS/OCTOSPIM_P1/SDMMC2/SWPMI1/TIM1x/TIM8/UART7/9/USART10	FMC/LCD/MDIOS/OCTOSPIM_P1/SDMMC1/TIM1x/TIM8	COMP/DCMI/PSSI/LCD/TIM1x/TIM23	LCD/TIM24/UART5	SYS
Port A	PA0	-	TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	TIM15_BKIN	SPI6_NSS/I2S6_WS	-	USART2_CTS/USART2_NSS	UART4_TX	SDMMC2_CMD	SAI4_SD_B	ETH_MII_CRS	FMC_A19	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	LPTIM3_OUT	TIM15_CH1N	-	-	USART2_RTS/USART2_DE	UART4_RX	OCTOSPIM_P1_IO3	SAI4_MCLK_B	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	OCTOSPIM_P1_DQS	-	LCD_R2	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	LPTIM4_OUT	TIM15_CH1	-	OCTOSPIM_P1_IO0	USART2_TX	SAI4_SCK_B	-	-	ETH_MDIO	MDIOS_MDIO	-	LCD_R1	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	LPTIM5_OUT	TIM15_CH2	I2S6_MCK	OCTOSPIM_P1_IO2	USART2_RX	-	LCD_B2	OTG_HS_ULPI_D0	ETH_MII_COL	OCTOSPIM_P1_CLK	-	LCD_B5	EVENTOUT
	PA4	D1PWREN	-	TIM5_ETR	-	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK	SPI6_NSS/I2S6_WS	-	-	-	FMC_D8/FMC_AD8	DCMI_HSYNC/PSSI_DE	LCD_VSYNC	EVENTOUT
	PA5	D2PWREN	TIM2_CH1/TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK/I2S1_CK	-	-	SPI6_SCK/I2S6_CK	-	OTG_HS_ULPI_CK	-	FMC_D9/FMC_AD9	PSSI_D14	LCD_R4	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO/I2S1_SDI	OCTOSPIM_P1_IO3	-	SPI6_MISO/I2S6_SDI	TIM13_CH1	TIM8_BKIN_COMP12	MDIOS_MDC	TIM1_BKIN_COMP12	DCMI_PIXCLK/PSSI_PDCK	LCD_G2	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI/I2S1_SDO	-	-	SPI6_MOSI/I2S6_SDO	TIM14_CH1	OCTOSPIM_P1_IO2	ETH_MII_RX_DV/ETH_RMII_CRS_DV	FMC_SDNWE	-	LCD_VSYNC	EVENTOUT

Table 8. STM32H733 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	FMC/LPTIM1/SAI4/TIM16/17/TIM1x/TIM2x	FDCAN3/PDM_SAI1/TIM3/4/5/12/15	DFSDM1/LCD/LPTIM2/3/4/5/LPUART1/OCTOSPIM_P1/2/TIM8	CEC/DCMI/PSSI/DFSDM1/I2C1/2/3/4/5/LPTIM2/OCTOSPIM_P1/TIM15/USART1/10	CEC/FDCAN3/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	DFSDM1/I2C4/5/OCTOSPIM_P1/SAI1/SPI3/I2S3/UART4	SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/UART7/USART1/2/3/6	LPUART1/SAI4/SDMMC1/SPDIFRX1/SPI6/UART4/5/8	FDCAN1/2/FMC/LCD/OCTOSPIM_P1/2/SAI4/SDMMC2/SPDIFRX1/TIM13/14	CRS/FMC/LCD/OCTOSPIM_P1/OTG1_FS/OTG1_HS/SAI4/SDMMC2/TIM8	DFSDM1/ETH/I2C4/LCD/MDIOS/OCTOSPIM_P1/SDMMC2/SWPMI1/TIM1x/TIM8/UART7/9/USART10	FMC/LCD/MDIOS/OCTOSPIM_P1/SDMMC1/TIM1x/TIM8	COMP/DCMI/PSSI/LCD/TIM1x/TIM23	LCD/TIM24/UART5	SYS
Port A	PA8	MCO1	TIM1_CH1	-	TIM8_BKIN2	I2C3_SCL	-	I2C5_SCL	USART1_CK	-	-	OTG_HS_SOF	UART7_RX	TIM8_BKIN2_COMP12	LCD_B3	LCD_R6	EVENTOUT
	PA9	-	TIM1_CH2	-	LPUART1_TX	I2C3_SMBA	SPI2_SCK/I2S2_CK	I2C5_SMBA	USART1_TX	-	-	-	ETH_TX_ER	-	DCMI_D0/PSSI_D0	LCD_R5	EVENTOUT
	PA10	-	TIM1_CH3	-	LPUART1_RX	-	-	-	USART1_RX	-	-	OTG_HS_ID	MDIOS_MDIO	LCD_B4	DCMI_D1/PSSI_D1	LCD_B1	EVENTOUT
	PA11	-	TIM1_CH4	-	LPUART1_CTS	-	SPI2_NSS/I2S2_WS	UART4_RX	USART1_CTS/USART1_NSS	-	FDCAN1_RX	-	-	-	-	LCD_R4	EVENTOUT
	PA12	-	TIM1_ETR	-	LPUART1_RTS/LPUART1_DE	-	SPI2_SCK/I2S2_CK	UART4_TX	USART1_RTS/USART1_DE	SAI4_FS_B	FDCAN1_TX	-	-	TIM1_BKIN2	-	LCD_R5	EVENTOUT
	PA13	JTMS/SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK/SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	-	-	CEC	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	SPI6_NSS/I2S6_WS	UART4_RTS/UART4_DE	LCD_R3	-	UART7_TX	-	-	LCD_B6	EVENTOUT

Table 8. STM32H733 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	FMC/LPTIM1/SAI4/TIM16/17/TIM1x/TIM2x	FDCAN3/PDM_SAI1/TIM3/4/5/12/15	DFSDM1/LCD/LPTIM2/3/4/5/LPUART1/OCTOSPIM_P1/2/TIM8	CEC/DCMI/PSSI/DFSDM1/I2C1/2/3/4/5/LPTIM2/OCTOSPIM_P1/TIM15/USART1/10	CEC/FDCAN3/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	DFSDM1/I2C4/5/OCTOSPIM_P1/SAI1/SPI3/I2S3/UART4	SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/UART7/USART1/2/3/6	LPUART1/SAI4/SDMMC1/SPDIFRX1/SPI6/UART4/5/8	FDCAN1/2/FMC/LCD/OCTOSPIM_P1/2/SAI4/SDMMC2/SPDIFRX1/TIM13/14	CRS/FMC/LCD/OCTOSPIM_P1/OTG1_FS/OTG1_HS/SAI4/SDMMC2/TIM8	DFSDM1/ETH/I2C4/LCD/MDIOS/OCTOSPIM_P1/SDMMC2/SWPMI1/TIM1x/TIM8/UART7/9/USART10	FMC/LCD/MDIOS/OCTOSPIM_P1/SDMMC1/TIM1x/TIM8	COMP/DCMI/PSSI/LCD/TIM1x/TIM23	LCD/TIM24/UART5	SYS
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	OCTOSPIM_P1_IO1	-	DFSDM1_CKOUT	-	UART4_CTS	LCD_R3	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	LCD_G1	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	OCTOSPIM_P1_IO0	-	DFSDM1_DATIN1	-	-	LCD_R6	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	LCD_G0	EVENTOUT
	PB2	RTC_OUT	SAI4_D1	SAI1_D1	-	DFSDM1_CKIN1	-	SAI1_SD_A	SPI3_MOSI/I2S3_SDO	SAI4_SD_A	OCTOSPIM_P1_CLK	OCTOSPIM_P1_DQS	ETH_TX_ER	-	TIM23_ETR	-	EVENTOUT
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	SPI6_SCK/I2S6_CK	SDMMC2_D2	CRS_SYNC	UART7_RX	-	-	TIM24_ETR	EVENTOUT
	PB4	NJTRST	TIM16_BKIN	TIM3_CH1	-	-	SPI1_MISO/I2S1_SDI	SPI3_MISO/I2S3_SDI	SPI2_NSS/I2S2_WS	SPI6_MISO/I2S6_SDI	SDMMC2_D3	-	UART7_TX	-	-	-	EVENTOUT
	PB5	-	TIM17_BKIN	TIM3_CH2	LCD_B5	I2C1_SMBA	SPI1_MOSI/I2S1_SDO	I2C4_SMBA	SPI3_MOSI/I2S3_SDO	SPI6_MOSI/I2S6_SDO	FDCAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	FMC_SDCKE1	DCMI_D10/PSSI_D10	UART5_RX	EVENTOUT
	PB6	-	TIM16_CH1N	TIM4_CH1	-	I2C1_SCL	CEC	I2C4_SCL	USART1_TX	LPUART1_TX	FDCAN2_TX	OCTOSPIM_P1_NCS	DFSDM1_DATIN5	FMC_SDNE1	DCMI_D5/PSSI_D5	UART5_TX	EVENTOUT
	PB7	-	TIM17_CH1N	TIM4_CH2	-	I2C1_SDA	-	I2C4_SDA	USART1_RX	LPUART1_RX	-	-	DFSDM1_CKIN5	FMC_NL	DCMI_VSYNC/PSSI_RDY	-	EVENTOUT
	PB8	-	TIM16_CH1	TIM4_CH3	DFSDM1_CKIN7	I2C1_SCL	-	I2C4_SCL	SDMMC1_CKIN	UART4_RX	FDCAN1_RX	SDMMC2_D4	ETH_MII_TXD3	SDMMC1_D4	DCMI_D6/PSSI_D6	LCD_B6	EVENTOUT
	PB9	-	TIM17_CH1	TIM4_CH4	DFSDM1_DATIN7	I2C1_SDA	SPI2_NSS/I2S2_WS	I2C4_SDA	SDMMC1_CDIR	UART4_TX	FDCAN1_TX	SDMMC2_D5	I2C4_SMBA	SDMMC1_D5	DCMI_D7/PSSI_D7	LCD_B7	EVENTOUT

Table 8. STM32H733 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	FMC/ LPTIM1/ SAI4/TIM16/17/TIM1x/TIM2x	FDCAN3/ PDM_ SAI1/ TIM3/4/5/12/15	DFSDM1/LCD/ LPTIM2/ 3/4/5/ LPUART1/OCTOSPIM_P1/2/TIM8	CEC/ DCMI/ PSSI/ DFSDM1/I2C1/2/3/ 4/5/ LPTIM2/ OCTOSPIM_P1/TIM15/ USART1/10	CEC/ FDCAN3/ SPI1/I2S1/SPI2/ I2S2/SPI3/I2S3/ SPI4/5/6	DFSDM1/I2C4/5/ OCTOSPIM_P1/ SAI1/ SPI3/ I2S3/ UART4	SDMMC1/SPI2/I2S2/SPI3/ I2S3/ SPI6/ UART7/ USART1/ 2/3/6	LPUART1/ SAI4/ SDMMC1/ SPDIFRX1/SPI6/ UART4/5/8	FDCAN1/2/FMC/ LCD/ OCTOSPIM_P1/ 2/SAI4/ SDMMC2/ SPDIFRX1/TIM13/14	CRS/ FMC/ LCD/ OCTOSPIM_P1/ OTG1_FS/ OTG1_HS/ SAI4/ SDMMC2/ TIM8	DFSDM1/ ETH/I2C4/ LCD/MDIOS/OCTOSPIM_P1/ SDMMC2/ SWPMI1/ TIM1x/TIM8/UART7/9/ USART10	FMC/LCD/ MDIOS/ OCTOSPIM_P1/ SDMMC1/ TIM1x/ TIM8	COMP/ DCMI/ PSSI/ LCD/ TIM1x/ TIM23	LCD/ TIM24/ UART5	SYS
Port B	PB10	-	TIM2_CH3	-	LPTIM2_IN1	I2C2_SCL	SPI2_SCK/ I2S2_CK	DFSDM1_DATIN7	USART3_TX	-	OCTOSPIM_P1_NCS	OTG_HS_ULPI_D3	ETH_MII_RX_ER	-	-	LCD_G4	EVENTOUT
	PB11	-	TIM2_CH4	-	LPTIM2_ETR	I2C2_SDA	-	DFSDM1_CKIN7	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH_MII_TX_EN/ ETH_RMII_TX_EN	-	-	LCD_G5	EVENTOUT
	PB12	-	TIM1_BKIN	-	OCTOSPIM_P1_NCLK	I2C2_SMBA	SPI2_NSS/ I2S2_WS	DFSDM1_DATIN1	USART3_CK	-	FDCAN2_RX	OTG_HS_ULPI_D5	ETH_MII_TXD0/ ETH_RMII_TXD0	OCTOSPIM_P1_IO0	TIM1_BKIN_COMP12	UART5_RX	EVENTOUT
	PB13	-	TIM1_CH1N	-	LPTIM2_OUT	OCTOSPIM_P1_IO2	SPI2_SCK/ I2S2_CK	DFSDM1_CKIN1	USART3_CTS/ USART3_NSS	-	FDCAN2_TX	OTG_HS_ULPI_D6	ETH_MII_TXD1/ ETH_RMII_TXD1	SDMMC1_D0	DCMI_D2/PSSI_D2	UART5_TX	EVENTOUT
	PB14	-	TIM1_CH2N	TIM12_CH1	TIM8_CH2N	USART1_TX	SPI2_MISO/ I2S2_SDI	DFSDM1_DATIN2	USART3_RTS/ USART3_DE	UART4_RTS/UART4_DE	SDMMC2_D0	-	-	FMC_D10/ FMC_AD10	-	LCD_CLK	EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	TIM12_CH2	TIM8_CH3N	USART1_RX	SPI2_MOSI/I2S2_SDO	DFSDM1_CKIN2	-	UART4_CTS	SDMMC2_D1	-	-	FMC_D11/ FMC_AD11	-	LCD_G7	EVENTOUT

Table 8. STM32H733 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	FMC/ LPTIM1/ SAI4/TIM16/17/TIM1x/TIM2x	FDCAN3/ PDM_ SAI1/ TIM3/4/5/12/15	DFSDM1/LCD/ LPTIM2/ 3/4/5/ LPUART1/OCTOSPIM_P1/2/TIM8	CEC/ DCMI/ PSSI/ DFSDM1/I2C1/2/3/4/5/ LPTIM2/ OCTOSPIM_P1/TIM15/ USART1/10	CEC/ FDCAN3/ SPI1/I2S1/SPI2/ I2S2/SPI3/I2S3/ SPI4/5/6	DFSDM1/I2C4/5/ OCTOSPIM_P1/ SAI1/ SPI3/ I2S3/ UART4	SDMMC1/SPI2/I2S2/SPI3/ I2S3/ SPI6/ UART7/ USART1/2/3/6	LPUART1/ SAI4/ SDMMC1/ SPDIFRX1/SPI6/ UART4/5/8	FDCAN1/2/FMC/ LCD/ OCTOSPIM_P1/2/SAI4/ SDMMC2/ SPDIFRX1/TIM13/14	CRS/ FMC/ LCD/ OCTOSPIM_P1/ OTG1_FS/ OTG1_HS/ SAI4/ SDMMC2/ TIM8	DFSDM1/ ETH/I2C4/ LCD/MDIOS/OCTOSPIM_P1/ SDMMC2/ SWPMI1/ TIM1x/TIM8/UART7/9/ USART10	FMC/LCD/ MDIOS/ OCTOSPIM_P1/ SDMMC1/ TIM1x/ TIM8	COMP/ DCMI/ PSSI/ LCD/ TIM1x/ TIM23	LCD/ TIM24/ UART5	SYS
Port C	PC0	-	FMC_D12/FMC_AD12	-	DFSDM1_CKIN0	-	-	DFSDM1_DATIN4	-	SAI4_FS_B	FMC_A25	OTG_HS_ULPI_STP	LCD_G2	FMC_SDNWE	-	LCD_R5	EVENTOUT
	PC1	TRACED0	SAI4_D1	SAI1_D1	DFSDM1_DATIN0	DFSDM1_CKIN4	SPI2_MOSI/I2S2_SDO	SAI1_SD_A	-	SAI4_SD_A	SDMMC2_CK	OCTOSPIM_P1_IO4	ETH_MDC	MDIOS_MDC	-	LCD_G5	EVENTOUT
	PC2	PWR_DEEPSLEEP	-	-	DFSDM1_CKIN1	OCTOSPIM_P1_IO5	SPI2_MISO/I2S2_SDI	DFSDM1_CKOUT	-	-	OCTOSPIM_P1_IO2	OTG_HS_ULPI_DIR	ETH_MII_TXD2	FMC_SDNE0	-	-	EVENTOUT
	PC3	PWR_SLEEP	-	-	DFSDM1_DATIN1	OCTOSPIM_P1_IO6	SPI2_MOSI/I2S2_SDO	-	-	-	OCTOSPIM_P1_IO0	OTG_HS_ULPI_NXT	ETH_MII_TX_CLK	FMC_SDCKE0	-	-	EVENTOUT
	PC4	PWR_DEEPSLEEP	FMC_A22	-	DFSDM1_CKIN2	-	I2S1_MCK	-	-	-	SPDIFRX1_IN3	SDMMC2_CKIN	ETH_MII_RXD0/ETH_RMII_RXD0	FMC_SDNE0	-	LCD_R7	EVENTOUT
	PC5	PWR_SLEEP	SAI4_D3	SAI1_D3	DFSDM1_DATIN2	PSSI_D15	-	-	-	-	SPDIFRX1_IN4	OCTOSPIM_P1_DQS	ETH_MII_RXD1/ETH_RMII_RXD1	FMC_SDCKE0	COMP1_OUT	LCD_DE	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	DFSDM1_CKIN3	I2S2_MCK	-	USART6_TX	SDMMC1_D0DIR	FMC_NWAIT	SDMMC2_D6	-	SDMMC1_D6	DCMI_D0/PSSI_D0	LCD_HSYNC	EVENTOUT
	PC7	DBTRGIO	-	TIM3_CH2	TIM8_CH2	DFSDM1_DATIN3	-	I2S3_MCK	USART6_RX	SDMMC1_D123DIR	FMC_NE1	SDMMC2_D7	SWPMI_TX	SDMMC1_D7	DCMI_D1/PSSI_D1	LCD_G6	EVENTOUT
	PC8	TRACED1	-	TIM3_CH3	TIM8_CH3	-	-	-	USART6_CK	UART5_RTS/UART5_DE	FMC_NE2/FMC_NCE	FMC_INT	SWPMI_RX	SDMMC1_D0	DCMI_D2/PSSI_D2	-	EVENTOUT

Table 8. STM32H733 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	FMC/LPTIM1/SAI4/TIM16/17/TIM1x/TIM2x	FDCAN3/PDM_SAI1/TIM3/4/5/12/15	DFSDM1/LCD/LPTIM2/3/4/5/LPUART1/OCTOSPIM_P1/2/TIM8	CEC/DCMI/PSSI/DFSDM1/I2C1/2/3/4/5/LPTIM2/OCTOSPIM_P1/TIM15/USART1/10	CEC/FDCAN3/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	DFSDM1/I2C4/5/OCTOSPIM_P1/SAI1/SPI3/I2S3/UART4	SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/UART7/USART1/2/3/6	LPUART1/SAI4/SDMMC1/SPDIFRX1/SPI6/UART4/5/8	FDCAN1/2/FMC/LCD/OCTOSPIM_P1/2/SAI4/SDMMC2/SPDIFRX1/TIM13/14	CRS/FMC/LCD/OCTOSPIM_P1/OTG1_FS/OTG1_HS/SAI4/SDMMC2/TIM8	DFSDM1/ETH/I2C4/LCD/MDIOS/OCTOSPIM_P1/SDMMC2/SWPMI1/TIM1x/TIM8/UART7/9/USART10	FMC/LCD/MDIOS/OCTOSPIM_P1/SDMMC1/TIM1x/TIM8	COMP/DCMI/PSSI/LCD/TIM1x/TIM23	LCD/TIM24/UART5	SYS
Port C	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN	I2C5_SDA	-	UART5_CTS	OCTOSPIM_P1_IO0	LCD_G3	SWPMI_SUSPEND	SDMMC1_D1	DCMI_D3/PSSI_D3	LCD_B2	EVENTOUT
	PC10	-	-	-	DFSDM1_CKIN5	I2C5_SDA	-	SPI3_SCK/I2S3_CK	USART3_TX	UART4_TX	OCTOSPIM_P1_IO1	LCD_B1	SWPMI_RX	SDMMC1_D2	DCMI_D8/PSSI_D8	LCD_R2	EVENTOUT
	PC11	-	-	-	DFSDM1_DATIN5	I2C5_SCL	-	SPI3_MISO/I2S3_SDI	USART3_RX	UART4_RX	OCTOSPIM_P1_NCS	-	-	SDMMC1_D3	DCMI_D4/PSSI_D4	LCD_B4	EVENTOUT
	PC12	TRACED3	FMC_D6/FMC_AD6	TIM15_CH1	-	I2C5_SMBA	SPI6_SCK/I2S6_CK	SPI3_MOSI/I2S3_SDO	USART3_CK	UART5_TX	-	-	-	SDMMC1_CK	DCMI_D9/PSSI_D9	LCD_R6	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 8. STM32H733 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	FMC/ LPTIM1/ SAI4/TIM16/17/TIM1x/TIM2x	FDCAN3/ PDM_SAI1/ TIM3/4/5/12/15	DFSDM1/LCD/ LPTIM2/3/4/5/ LPUART1/OCTOSPIM_P1/2/TIM8	CEC/ DCMI/ PSSI/ DFSDM1/I2C1/2/3/4/5/ LPTIM2/ OCTOSPIM_P1/TIM15/ USART1/10	CEC/ FDCAN3/ SPI1/I2S1/SPI2/ I2S2/SPI3/I2S3/ SPI4/5/6	DFSDM1/I2C4/5/ OCTOSPIM_P1/ SAI1/ SPI3/ I2S3/ UART4	SDMMC1/SPI2/I2S2/SPI3/ I2S3/ SPI6/ UART7/ USART1/2/3/6	LPUART1/ SAI4/ SDMMC1/ SPDIFRX1/SPI6/ UART4/5/8	FDCAN1/2/FMC/ LCD/ OCTOSPIM_P1/2/SAI4/ SDMMC2/ SPDIFRX1/TIM13/14	CRS/ FMC/ LCD/ OCTOSPIM_P1/ OTG1_FS/ OTG1_HS/ SAI4/ SDMMC2/ TIM8	DFSDM1/ ETH/I2C4/ LCD/MDIOS/OCTOSPIM_P1/ SDMMC2/ SWPMI1/ TIM1x/TIM8/UART7/9/ USART10	FMC/LCD/ MDIOS/ OCTOSPIM_P1/ SDMMC1/ TIM1x/ TIM8	COMP/ DCMI/ PSSI/ LCD/ TIM1x/ TIM23	LCD/ TIM24/ UART5	SYS
Port D	PD0	-	-	-	DFSDM1_CKIN6	-	-	-	-	UART4_RX	FDCAN1_RX	-	UART9_CTS	FMC_D2/ FMC_AD2	-	LCD_B1	EVENTOUT
	PD1	-	-	-	DFSDM1_DATIN6	-	-	-	-	UART4_TX	FDCAN1_TX	-	-	FMC_D3/ FMC_AD3	-	-	EVENTOUT
	PD2	TRACED2	FMC_D7/ FMC_AD7	TIM3_ETR	-	TIM15_BKIN	-	-	-	UART5_RX	LCD_B7	-	-	SDMMC1_CMD	DCMI_D11/PSSI_D11	LCD_B2	EVENTOUT
	PD3	-	-	-	DFSDM1_CKOUT	-	SPI2_SCK/ I2S2_CK	-	USART2_CTS/ USART2_NSS	-	-	-	-	FMC_CLK	DCMI_D5/PSSI_D5	LCD_G7	EVENTOUT
	PD4	-	-	-	-	-	-	-	USART2_RTS/ USART2_DE	-	-	OCTOSPIM_P1_IO4	-	FMC_NOE	-	-	EVENTOUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	OCTOSPIM_P1_IO5	-	FMC_NWE	-	-	EVENTOUT
	PD6	-	SAI4_D1	SAI1_D1	DFSDM1_CKIN4	DFSDM1_DATIN1	SPI3_MOSI/I2S3_SDO	SAI1_SD_A	USART2_RX	SAI4_SD_A	-	OCTOSPIM_P1_IO6	SDMMC2_CK	FMC_NWAIT	DCMI_D10/PSSI_D10	LCD_B2	EVENTOUT
	PD7	-	-	-	DFSDM1_DATIN4	-	SPI1_MOSI/I2S1_SDO	DFSDM1_CKIN1	USART2_CK	-	SPDIFRX1_IN1	OCTOSPIM_P1_IO7	SDMMC2_CMD	FMC_NE1	-	-	EVENTOUT
	PD8	-	-	-	DFSDM1_CKIN3	-	-	-	USART3_TX	-	SPDIFRX1_IN2	-	-	FMC_D13/ FMC_AD13	-	-	EVENTOUT

Table 8. STM32H733 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	FMC/LPTIM1/SAI4/TIM16/17/TIM1x/TIM2x	FDCAN3/PDM_SAI1/TIM3/4/5/12/15	DFSDM1/LCD/LPTIM2/3/4/5/LPUART1/OCTOSPIM_P1/2/TIM8	CEC/DCMI/PSSI/DFSDM1/I2C1/2/3/4/5/LPTIM2/OCTOSPIM_P1/TIM15/USART1/10	CEC/FDCAN3/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	DFSDM1/I2C4/5/OCTOSPIM_P1/SAI1/SPI3/I2S3/UART4	SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/UART7/USART1/2/3/6	LPUART1/SAI4/SDMMC1/SPDIFRX1/SPI6/UART4/5/8	FDCAN1/2/FMC/LCD/OCTOSPIM_P1/2/SAI4/SDMMC2/SPDIFRX1/TIM13/14	CRS/FMC/LCD/OCTOSPIM_P1/OTG1_FS/OTG1_HS/SAI4/SDMMC2/TIM8	DFSDM1/ETH/I2C4/LCD/MDIOS/OCTOSPIM_P1/SDMMC2/SWPMI1/TIM1x/TIM8/UART7/9/USART10	FMC/LCD/MDIOS/OCTOSPIM_P1/SDMMC1/TIM1x/TIM8	COMP/DCMI/PSSI/LCD/TIM1x/TIM23	LCD/TIM24/UART5	SYS
Port D	PD9	-	-	-	DFSDM1_DATIN3	-	-	-	USART3_RX	-	-	-	-	FMC_D14/FMC_AD14	-	-	EVENTOUT
Port D	PD10	-	-	-	DFSDM1_CKOUT	-	-	-	USART3_CK	-	-	-	-	FMC_D15/FMC_AD15	-	LCD_B3	EVENTOUT
Port D	PD11	-	-	-	LPTIM2_IN2	I2C4_SMBA	-	-	USART3_CTS/USART3_NSS	-	OCTOSPIM_P1_IO0	SAI4_SD_A	-	FMC_A16/FMC_CLE	-	-	EVENTOUT
Port D	PD12	-	LPTIM1_IN1	TIM4_CH1	LPTIM2_IN1	I2C4_SCL	FDCAN3_RX	-	USART3_RTS/USART3_DE	-	OCTOSPIM_P1_IO1	SAI4_FS_A	-	FMC_A17/FMC_ALE	DCMI_D12/PSSI_D12	-	EVENTOUT
Port D	PD13	-	LPTIM1_OUT	TIM4_CH2	-	I2C4_SDA	FDCAN3_TX	-	-	-	OCTOSPIM_P1_IO3	SAI4_SCK_A	UART9_RTS/UART9_DE	FMC_A18	DCMI_D13/PSSI_D13	-	EVENTOUT
Port D	PD14	-	-	TIM4_CH3	-	-	-	-	-	UART8_CTS	-	-	UART9_RX	FMC_D0/FMC_AD0	-	-	EVENTOUT
Port D	PD15	-	-	TIM4_CH4	-	-	-	-	-	UART8_RTS/UART8_DE	-	-	UART9_TX	FMC_D1/FMC_AD1	-	-	EVENTOUT

Table 8. STM32H733 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	FMC/LPTIM1/SAI4/TIM16/17/TIM1x/TIM2x	FDCAN3/PDM_SAI1/TIM3/4/5/12/15	DFSDM1/LCD/LPTIM2/3/4/5/LPUART1/OCTOSPIM_P1/2/TIM8	CEC/DCMI/PSSI/DFSDM1/I2C1/2/3/4/5/LPTIM2/OCTOSPIM_P1/TIM15/USART1/10	CEC/FDCAN3/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	DFSDM1/I2C4/5/OCTOSPIM_P1/SAI1/SPI3/I2S3/UART4	SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/UART7/USART1/2/3/6	LPUART1/SAI4/SDMMC1/SPDIFRX1/SPI6/UART4/5/8	FDCAN1/2/FMC/LCD/OCTOSPIM_P1/2/SAI4/SDMMC2/SPDIFRX1/TIM13/14	CRS/FMC/LCD/OCTOSPIM_P1/OTG1_FS/OTG1_HS/SAI4/SDMMC2/TIM8	DFSDM1/ETH/I2C4/LCD/MDIOS/OCTOSPIM_P1/SDMMC2/SWPMI1/TIM1x/TIM8/UART7/9/USART10	FMC/LCD/MDIOS/OCTOSPIM_P1/SDMMC1/TIM1x/TIM8	COMP/DCMI/PSSI/LCD/TIM1x/TIM23	LCD/TIM24/UART5	SYS
Port E	PE0	-	LPTIM1_ETR	TIM4_ETR	-	LPTIM2_ETR	-	-	-	UART8_RX	-	SAI4_MCLK_A	-	FMC_NBL0	DCMI_D2/PSSI_D2	LCD_R0	EVENTOUT
	PE1	-	LPTIM1_IN2	-	-	-	-	-	-	UART8_TX	-	-	-	FMC_NBL1	DCMI_D3/PSSI_D3	LCD_R6	EVENTOUT
	PE2	TRACECLK	-	SAI1_CK1	-	USART10_RX	SPI4_SCK	SAI1_MCLK_A	-	SAI4_MCLK_A	OCTOSPIM_P1_IO2	SAI4_CK1	ETH_MII_TXD3	FMC_A23	-	-	EVENTOUT
	PE3	TRACED0	-	-	-	TIM15_BKIN	-	SAI1_SD_B	-	SAI4_SD_B	-	-	USART10_TX	FMC_A19	-	-	EVENTOUT
	PE4	TRACED1	-	SAI1_D2	DFSDM1_DATIN3	TIM15_CH1N	SPI4_NSS	SAI1_FS_A	-	SAI4_FS_A	-	SAI4_D2	-	FMC_A20	DCMI_D4/PSSI_D4	LCD_B0	EVENTOUT
	PE5	TRACED2	-	SAI1_CK2	DFSDM1_CKIN3	TIM15_CH1	SPI4_MISO	SAI1_SCK_A	-	SAI4_SCK_A	-	SAI4_CK2	-	FMC_A21	DCMI_D6/PSSI_D6	LCD_G0	EVENTOUT
	PE6	TRACED3	TIM1_BKIN2	SAI1_D1	-	TIM15_CH2	SPI4_MOSI	SAI1_SD_A	-	SAI4_SD_A	SAI4_D1	SAI4_MCLK_B	TIM1_BKIN2_COMP12	FMC_A22	DCMI_D7/PSSI_D7	LCD_G1	EVENTOUT
	PE7	-	TIM1_ETR	-	DFSDM1_DATIN2	-	-	-	UART7_RX	-	-	OCTOSPIM_P1_IO4	-	FMC_D4/FMC_AD4	-	-	EVENTOUT
	PE8	-	TIM1_CH1N	-	DFSDM1_CKIN2	-	-	-	UART7_TX	-	-	OCTOSPIM_P1_IO5	-	FMC_D5/FMC_AD5	COMP2_OUT	-	EVENTOUT
	PE9	-	TIM1_CH1	-	DFSDM1_CKOUT	-	-	-	UART7_RTS/UART7_DE	-	-	OCTOSPIM_P1_IO6	-	FMC_D6/FMC_AD6	-	-	EVENTOUT

Table 8. STM32H733 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	FMC/ LPTIM1/ SAI4/TIM16/17/TIM1x/TIM2x	FDCAN3/ PDM_ SAI1/ TIM3/4/5/12/15	DFSDM1/LCD/ LPTIM2/3/4/5/ LPUART1/OCTOSPIM_P1/2/TIM8	CEC/ DCMI/ PSSI/ DFSDM1/I2C1/2/3/4/5/ LPTIM2/ OCTOSPIM_P1/TIM15/ USART1/10	CEC/ FDCAN3/ SPI1/I2S1/SPI2/ I2S2/SPI3/I2S3/ SPI4/5/6	DFSDM1/I2C4/5/ OCTOSPIM_P1/ SAI1/ SPI3/ I2S3/ UART4	SDMMC1/SPI2/I2S2/SPI3/ I2S3/ SPI6/ UART7/ USART1/2/3/6	LPUART1/ SAI4/ SDMMC1/ SPDIFRX1/SPI6/ UART4/5/8	FDCAN1/2/FMC/ LCD/ OCTOSPIM_P1/2/SAI4/ SDMMC2/ SPDIFRX1/TIM13/14	CRS/ FMC/ LCD/ OCTOSPIM_P1/ OTG1_FS/ OTG1_HS/ SAI4/ SDMMC2/ TIM8	DFSDM1/ ETH/I2C4/ LCD/MDIOS/OCTOSPIM_P1/ SDMMC2/ SWPMI1/ TIM1x/TIM8/UART7/9/ USART10	FMC/LCD/ MDIOS/ OCTOSPIM_P1/ SDMMC1/ TIM1x/ TIM8	COMP/ DCMI/ PSSI/ LCD/ TIM1x/ TIM23	LCD/ TIM24/ UART5	SYS
Port E	PE10	-	TIM1_CH2N	-	DFSDM1_DATIN4	-	-	-	UART7_CTS	-	-	OCTOSPIM_P1_IO7	-	FMC_D7/FMC_AD7	-	-	EVENTOUT
	PE11	-	TIM1_CH2	-	DFSDM1_CKIN4	-	SPI4_NSS	-	-	-	-	SAI4_SD_B	OCTOSPIM_P1_NCS	FMC_D8/FMC_AD8	-	LCD_G3	EVENTOUT
	PE12	-	TIM1_CH3N	-	DFSDM1_DATIN5	-	SPI4_SCK	-	-	-	-	SAI4_SCK_B	-	FMC_D9/FMC_AD9	COMP1_OUT	LCD_B4	EVENTOUT
	PE13	-	TIM1_CH3	-	DFSDM1_CKIN5	-	SPI4_MISO	-	-	-	-	SAI4_FS_B	-	FMC_D10/FMC_AD10	COMP2_OUT	LCD_DE	EVENTOUT
	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI	-	-	-	-	SAI4_MCLK_B	-	FMC_D11/FMC_AD11	-	LCD_CLK	EVENTOUT
	PE15	-	TIM1_BKIN	-	-	-	-	-	-	-	-	-	USART10_CK	FMC_D12/FMC_AD12	TIM1_BKIN_COMP12	LCD_R7	EVENTOUT

Table 8. STM32H733 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	FMC/ LPTIM1/ SAI4/TIM16/17/TIM1x/TIM2x	FDCAN3/ PDM_ SAI1/ TIM3/4/5/12/15	DFSDM1/LCD/ LPTIM2/ 3/4/5/ LPUART1/OCTOSPIM_P1/2/TIM8	CEC/ DCMI/ PSSI/ DFSDM1/I2C1/2/3/4/5/ LPTIM2/ OCTOSPIM_P1/TIM15/ USART1/10	CEC/ FDCAN3/ SPI1/I2S1/SPI2/ I2S2/SPI3/I2S3/ SPI4/5/6	DFSDM1/I2C4/5/ OCTOSPIM_P1/ SAI1/ SPI3/ I2S3/ UART4	SDMMC1/SPI2/I2S2/SPI3/ I2S3/ SPI6/ UART7/ USART1/2/3/6	LPUART1/ SAI4/ SDMMC1/ SPDIFRX1/SPI6/ UART4/5/8	FDCAN1/2/FMC/ LCD/ OCTOSPIM_P1/2/SAI4/ SDMMC2/ SPDIFRX1/TIM13/14	CRS/ FMC/ LCD/ OCTOSPIM_P1/ OTG1_FS/ OTG1_HS/ SAI4/ SDMMC2/ TIM8	DFSDM1/ ETH/I2C4/ LCD/MDIOS/OCTOSPIM_P1/ SDMMC2/ SWPMI1/ TIM1x/TIM8/UART7/9/ USART10	FMC/LCD/ MDIOS/ OCTOSPIM_P1/ SDMMC1/ TIM1x/ TIM8	COMP/ DCMI/ PSSI/ LCD/ TIM1x/ TIM23	LCD/ TIM24/ UART5	SYS
Port F	PF0	-	-	-	-	I2C2_ SDA	-	I2C5_SDA	-	-	OCTOSPIM_P2_IO0	-	-	FMC_A0	TIM23_ CH1	-	EVENTOUT
Port F	PF1	-	-	-	-	I2C2_ SCL	-	I2C5_SCL	-	-	OCTOSPIM_P2_IO1	-	-	FMC_A1	TIM23_ CH2	-	EVENTOUT
Port F	PF2	-	-	-	-	I2C2_ SMBA	-	I2C5_ SMBA	-	-	OCTOSPIM_P2_IO2	-	-	FMC_A2	TIM23_ CH3	-	EVENTOUT
Port F	PF3	-	-	-	-	-	-	-	-	-	OCTOSPIM_P2_IO3	-	-	FMC_A3	TIM23_ CH4	-	EVENTOUT
Port F	PF4	-	-	-	-	-	-	-	-	-	OCTOSPIM_P2_CLK	-	-	FMC_A4	-	-	EVENTOUT
Port F	PF5	-	-	-	-	-	-	-	-	-	OCTOSPIM_P2_NCLK	-	-	FMC_A5	-	-	EVENTOUT
Port F	PF6	-	TIM16_ CH1	FDCAN3_ RX	-	-	SPI5_ NSS	SAI1_SD_ B	UART7_ RX	SAI4_SD_ B	-	OCTOSPIM_P1_IO3	-	-	TIM23_ CH1	-	EVENTOUT
Port F	PF7	-	TIM17_ CH1	FDCAN3_ TX	-	-	SPI5_ SCK	SAI1_ MCLK_B	UART7_ TX	SAI4_ MCLK_B	-	OCTOSPIM_P1_IO2	-	-	TIM23_ CH2	-	EVENTOUT
Port F	PF8	-	TIM16_ CH1N	-	-	-	SPI5_ MISO	SAI1_SCK _B	UART7_ RTS/ UART7_ DE	SAI4_SCK _B	TIM13_CH 1	OCTOSPIM_P1_IO0	-	-	TIM23_ CH3	-	EVENTOUT
Port F	PF9	-	TIM17_ CH1N	-	-	-	SPI5_ MOSI	SAI1_FS_ B	UART7_ CTS	SAI4_FS_ B	TIM14_CH 1	OCTOSPIM_P1_IO1	-	-	TIM23_ CH4	-	EVENTOUT

Table 8. STM32H733 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	FMC/ LPTIM1/ SAI4/TIM16/17/TIM1x/TIM2x	FDCAN3/ PDM_ SAI1/ TIM3/4/5/12/15	DFSDM1/LCD/ LPTIM2/3/4/5/ LPUART1/OCTOSPIM_P1/2/TIM8	CEC/ DCMI/ PSSI/ DFSDM1/I2C1/2/3/4/5/ LPTIM2/ OCTOSPIM_P1/TIM15/ USART1/10	CEC/ FDCAN3/ SPI1/I2S1/SPI2/ I2S2/SPI3/I2S3/ SPI4/5/6	DFSDM1/I2C4/5/ OCTOSPIM_P1/ SAI1/ SPI3/ I2S3/ UART4	SDMMC1/SPI2/I2S2/SPI3/ I2S3/ SPI6/ UART7/ USART1/2/3/6	LPUART1/ SAI4/ SDMMC1/ SPDIFRX1/SPI6/ UART4/5/8	FDCAN1/2/FMC/ LCD/ OCTOSPIM_P1/2/SAI4/ SDMMC2/ SPDIFRX1/TIM13/14	CRS/ FMC/ LCD/ OCTOSPIM_P1/ OTG1_FS/ OTG1_HS/ SAI4/ SDMMC2/ TIM8	DFSDM1/ ETH/I2C4/ LCD/MDIOS/OCTOSPIM_P1/ SDMMC2/ SWPMI1/ TIM1x/TIM8/UART7/9/ USART10	FMC/LCD/ MDIOS/ OCTOSPIM_P1/ SDMMC1/ TIM1x/ TIM8	COMP/ DCMI/ PSSI/ LCD/ TIM1x/ TIM23	LCD/ TIM24/ UART5	SYS
Port F	PF10	-	TIM16_BKIN	SAI1_D3	-	PSSI_D15	-	-	-	-	OCTOSPIM_P1_CLK	SAI4_D3	-	-	DCMI_D11/PSSI_D11	LCD_DE	EVENTOUT
	PF11	-	-	-	-	-	SPI5_MOSI	-	-	-	OCTOSPIM_P1_NCLK	SAI4_SD_B	-	FMC_NRAS	DCMI_D12/PSSI_D12	TIM24_CH1	EVENTOUT
	PF12	-	-	-	-	-	-	-	-	-	OCTOSPIM_P2_DQS	-	-	FMC_A6	-	TIM24_CH2	EVENTOUT
	PF13	-	-	-	DFSDM1_DATIN6	I2C4_SMBA	-	-	-	-	-	-	-	FMC_A7	-	TIM24_CH3	EVENTOUT
	PF14	-	-	-	DFSDM1_CKIN6	I2C4_SCL	-	-	-	-	-	-	-	FMC_A8	-	TIM24_CH4	EVENTOUT
	PF15	-	-	-	-	I2C4_SDA	-	-	-	-	-	-	-	FMC_A9	-	-	EVENTOUT

Table 8. STM32H733 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	FMC/ LPTIM1/ SAI4/TIM16/17/TIM1x/TIM2x	FDCAN3/ PDM_ SAI1/ TIM3/4/5/12/15	DFSDM1/LCD/ LPTIM2/ 3/4/5/ LPUART1/OCTOSPIM_P1/2/TIM8	CEC/ DCMI/ PSSI/ DFSDM1/I2C1/2/3/4/5/ LPTIM2/ OCTOSPIM_P1/TIM15/ USART1/10	CEC/ FDCAN3/ SPI1/I2S1/SPI2/ I2S2/SPI3/I2S3/ SPI4/5/6	DFSDM1/I2C4/5/ OCTOSPIM_P1/ SAI1/ SPI3/ I2S3/ UART4	SDMMC1/SPI2/I2S2/SPI3/ I2S3/ SPI6/ UART7/ USART1/2/3/6	LPUART1/ SAI4/ SDMMC1/ SPDIFRX1/SPI6/ UART4/5/8	FDCAN1/2/FMC/ LCD/ OCTOSPIM_P1/2/SAI4/ SDMMC2/ SPDIFRX1/TIM13/14	CRS/ FMC/ LCD/ OCTOSPIM_P1/ OTG1_FS/ OTG1_HS/ SAI4/ SDMMC2/ TIM8	DFSDM1/ ETH/I2C4/ LCD/MDIOS/OCTOSPIM_P1/ SDMMC2/ SWPMI1/ TIM1x/TIM8/UART7/9/ USART10	FMC/LCD/ MDIOS/ OCTOSPIM_P1/ SDMMC1/ TIM1x/ TIM8	COMP/ DCMI/ PSSI/ LCD/ TIM1x/ TIM23	LCD/ TIM24/ UART5	SYS
Port G	PG0	-	-	-	-	-	-	-	-	-	OCTOSPIM_P2_IO4	-	UART9_RX	FMC_A10	-	-	EVENTOUT
Port G	PG1	-	-	-	-	-	-	-	-	-	OCTOSPIM_P2_IO5	-	UART9_TX	FMC_A11	-	-	EVENTOUT
Port G	PG2	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	TIM8_BKIN_COMP12	FMC_A12	-	TIM24_ETR	EVENTOUT
Port G	PG3	-	-	-	TIM8_BKIN2	-	-	-	-	-	-	-	TIM8_BKIN2_COMP12	FMC_A13	TIM23_ETR	-	EVENTOUT
Port G	PG4	-	TIM1_BKIN2	-	-	-	-	-	-	-	-	-	TIM1_BKIN2_COMP12	FMC_A14/FMC_BA0	-	-	EVENTOUT
Port G	PG5	-	TIM1_ETR	-	-	-	-	-	-	-	-	-	-	FMC_A15/FMC_BA1	-	-	EVENTOUT
Port G	PG6	-	TIM17_BKIN	-	-	-	-	-	-	-	-	OCTOSPIM_P1_NCS	-	FMC_NE3	DCMI_D12/PSSI_D12	LCD_R7	EVENTOUT
Port G	PG7	-	-	-	-	-	-	SAI1_MCLK_A	USART6_CK	-	OCTOSPIM_P2_DQS	-	-	FMC_INT	DCMI_D13/PSSI_D13	LCD_CLK	EVENTOUT
Port G	PG8	-	-	-	TIM8_ETR	-	SPI6_NSS/I2S6_WS	-	USART6_RTS/USART6_DE	SPDIFRX1_IN3	-	-	ETH_PPS_OUT	FMC_SDCLK	-	LCD_G7	EVENTOUT
Port G	PG9	-	-	FDCAN3_TX	-	-	SPI1_MISO/I2S1_SDI	-	USART6_RX	SPDIFRX1_IN4	OCTOSPIM_P1_IO6	SAI4_FS_B	SDMMC2_D0	FMC_NE2/FMC_NCE	DCMI_VSYNC/PSSI_RDY	-	EVENTOUT

Table 8. STM32H733 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	FMC/LPTIM1/SAI4/TIM16/17/TIM1x/TIM2x	FDCAN3/PDM_SAI1/TIM3/4/5/12/15	DFSDM1/LCD/LPTIM2/3/4/5/LPUART1/OCTOSPIM_P1/2/TIM8	CEC/DCMI/PSSI/DFSDM1/I2C1/2/3/4/5/LPTIM2/OCTOSPIM_P1/TIM15/USART1/10	CEC/FDCAN3/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	DFSDM1/I2C4/5/OCTOSPIM_P1/SAI1/SPI3/I2S3/UART4	SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/UART7/USART1/2/3/6	LPUART1/SAI4/SDMMC1/SPDIFRX1/SPI6/UART4/5/8	FDCAN1/2/FMC/LCD/OCTOSPIM_P1/2/SAI4/SDMMC2/SPDIFRX1/TIM13/14	CRS/FMC/LCD/OCTOSPIM_P1/OTG1_FS/OTG1_HS/SAI4/SDMMC2/TIM8	DFSDM1/ETH/I2C4/LCD/MDIOS/OCTOSPIM_P1/SDMMC2/SWPMI1/TIM1x/TIM8/UART7/9/USART10	FMC/LCD/MDIOS/OCTOSPIM_P1/SDMMC1/TIM1x/TIM8	COMP/DCMI/PSSI/LCD/TIM1x/TIM23	LCD/TIM24/UART5	SYS
Port G	PG10	-	-	FDCAN3_RX	OCTOSPIM_P2_IO6	-	SPI1_NSS/I2S1_WS	-	-	-	LCD_G3	SAI4_SD_B	SDMMC2_D1	FMC_NE3	DCMI_D2/PSSI_D2	LCD_B2	EVENTOUT
	PG11	-	LPTIM1_IN2	-	-	USART10_RX	SPI1_SCK/I2S1_CK	-	-	SPDIFRX1_IN1	OCTOSPIM_P2_IO7	SDMMC2_D2	ETH_MII_TX_EN/ETH_RMII_TX_EN	-	DCMI_D3/PSSI_D3	LCD_B3	EVENTOUT
	PG12	-	LPTIM1_IN1	-	OCTOSPIM_P2_NCS	USART10_TX	SPI6_MISO/I2S6_SDI	-	USART6_RTS/USART6_DE	SPDIFRX1_IN2	LCD_B4	SDMMC2_D3	ETH_MII_TXD1/ETH_RMII_TXD1	FMC_NE4	TIM23_CH1	LCD_B1	EVENTOUT
	PG13	TRACED0	LPTIM1_OUT	-	-	USART10_CTS/USART10_NSS	SPI6_SCK/I2S6_CK	-	USART6_CTS/USART6_NSS	-	-	SDMMC2_D6	ETH_MII_TXD0/ETH_RMII_TXD0	FMC_A24	TIM23_CH2	LCD_R0	EVENTOUT
	PG14	TRACED1	LPTIM1_ETR	-	-	USART10_RTS/USART10_DE	SPI6_MOSI/I2S6_SDO	-	USART6_TX	-	OCTOSPIM_P1_IO7	SDMMC2_D7	ETH_MII_TXD1/ETH_RMII_TXD1	FMC_A25	TIM23_CH3	LCD_B0	EVENTOUT
	PG15	-	-	-	-	-	-	-	USART6_CTS/USART6_NSS	-	OCTOSPIM_P2_DQS	-	USART10_CK	FMC_NCAS	DCMI_D13/PSSI_D13	-	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100% of the devices with a junction temperature at T_J = 25 °C and $T_J = T_{Jmax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, V_{DD} = 3.3 V (for the 1.7 V $\leq V_{DD} \leq$ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 8. Pin loading conditions

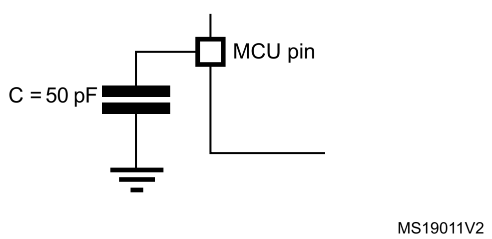
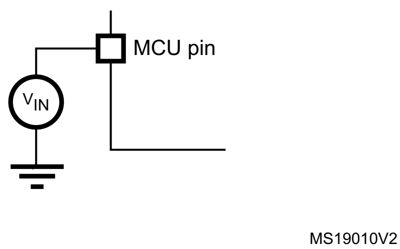
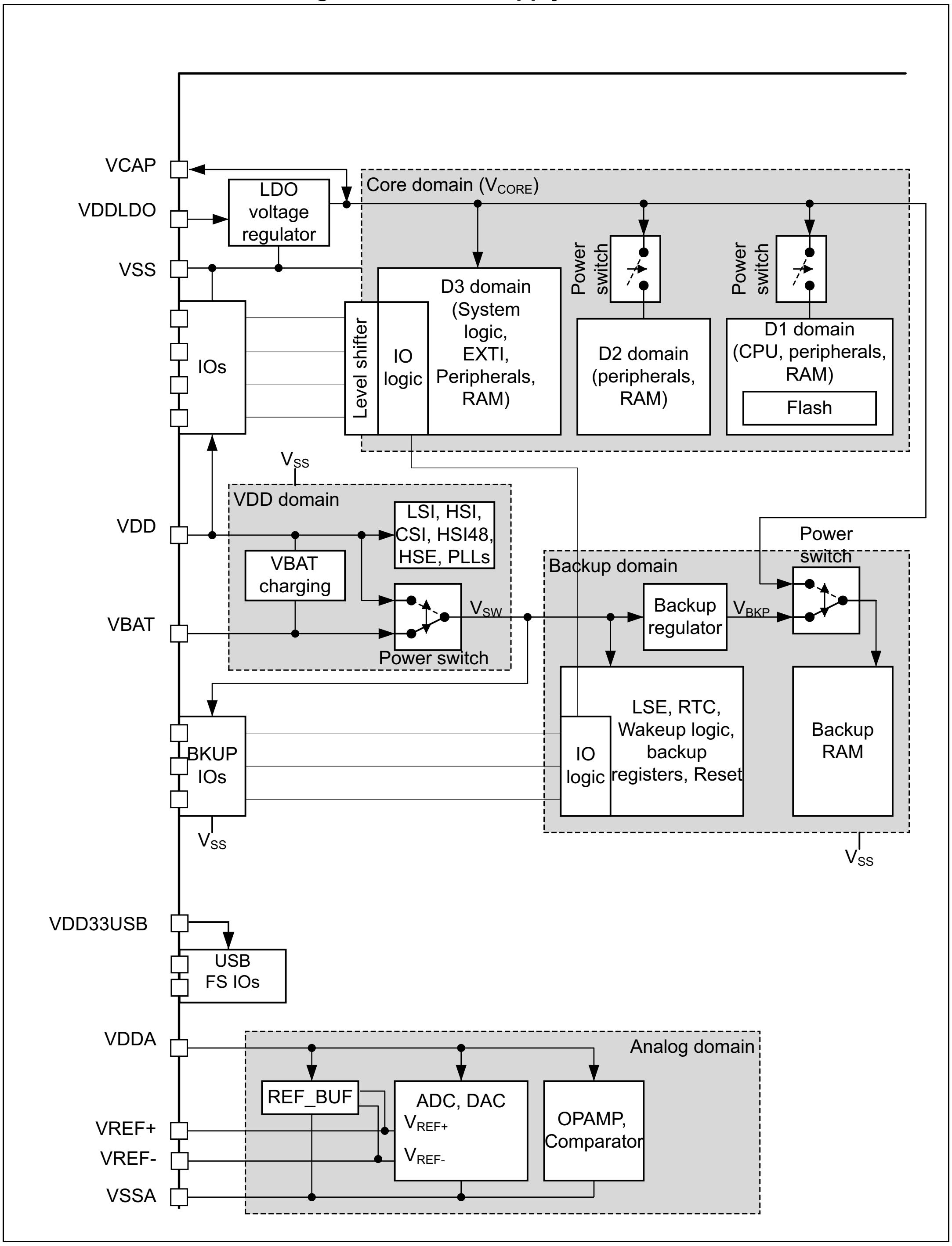


Figure 9. Pin input voltage



6.1.6 Power supply scheme

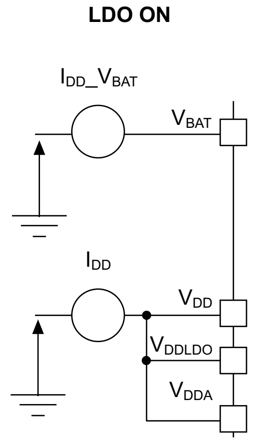
Figure 10. Power supply scheme



1. Refer to application note AN5419 "*Getting started with STM32H723/733, STM32H725/735 and STM32H730 Value Line hardware development*" for the possible power scheme and connected capacitors.

6.1.7 Current consumption measurement

Figure 11. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 9: Voltage characteristics*, *Table 10: Current characteristics*, and *Table 11: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Note: For information on product lifetime estimation, refer to application note AN5337: Guidelines for estimating STM32H7 MCUs lifetime, available from the STMicroelectronics website www.st.com.

Table 9. Voltage characteristics

Symbols	Ratings	Min	Max	Unit
$V_{DDX} - V_{SS}$(1)	External main supply voltage (including V_{DD}, V_{DDLDO}, V_{DDA}, $V_{DD33USB}$, V_{BAT})	−0.3	4.0	V
V_{IN}(2)	Input voltage on FT_xxx pins	$V_{SS}-0.3$	Min(V_{DD}, V_{DDA}, $V_{DD33USB}$, V_{BAT}) +4.0(3)(4)	V
	Input voltage on TT_xx pins	$V_{SS}-0.3$	4.0	V
	Input voltage on BOOT0 pin	V_{SS}	9.0	V
	Input voltage on any other pins	V_{SS}-0.3	4.0	V
$\lvert\Delta V_{DDX}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV

1. All main power (V_{DD}, V_{DDA}, $V_{DD33USB}$, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 50: I/O current injection susceptibility* for the maximum allowed injected current values.
3. This formula has to be applied on power supplies related to the IO structure described by the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.

Table 10. Current characteristics

Symbols	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	620	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	620	
IV_{DD}	Maximum current into each V_{DD} power pin (source)(1)	100	
IV_{SS}	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
I_{IO}	Output current sunk or sourced by any I/O and control pin, except Pxy_C	20	
	Output current sunk or sourced by Pxy_C pins	1	
$\Sigma I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	140	
	Total output current sourced by sum of all I/Os and control pins(2)	140	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xxx, TT_xx, RST and B pins except PA4, PA5	−5/+0	
	Injected current on PA4, PA5	−0/0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}, $V_{DD33USB}$) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 9: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 11. Thermal characteristics

Symbol	Ratings		Value	Unit
T_{STG}	Storage temperature range		− 65 to +150	°C
T_J	Maximum junction temperature	Industrial temperature range 6	125	

6.3 Operating conditions

6.3.1 General operating conditions

Table 12. General operating conditions

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{DD}	Standard operating voltage	-	1.62[1]	-	3.6	
V_{DDLDO}	Supply voltage for the internal regulator	$V_{DDLDO} \leq V_{DD}$	1.62[1]	-	3.6	
$V_{DD33USB}$	Standard operating voltage, USB domain	USB used	3.0	-	3.6	
		USB not used	0	-	3.6	
V_{DDA}	Analog operating voltage	ADC or COMP used	1.62	-	3.6	
		DAC used	1.8	-		
		OPAMP used	2.0	-		
		VREFBUF used	1.8	-		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0	-		
V_{BAT}	Supply voltage for Backup domain	-	1.2[2]	-	3.6	V
V_{IN}	I/O Input voltage	TT_xx I/O except Pxy_C	−0.3	-	V_{DD}+0.3	
		Pxy_C I/O	−0.3	-	Min(V_{DDA}, V_{DD}) + 0.3	
		BOOT0	0	-	9	
		All I/Os except BOOT0, TT_xx and Pxy_C	−0.3	-	Min(V_{DD}, V_{DDA}, $V_{DD33USB}$) + 3.6 < 5.5[3]	
V_{CORE}	Internal regulator ON (LDO)[4]	VOS3	0.95	1.0	1.05	V
		VOS2	1.05	1.10	1.15	
		VOS1	1.15	1.21	1.26	
		VOS0	1.30	1.36	1.40	
	Regulator OFF: external V_{CORE} voltage must be supplied from external regulator on VCAP pins	VOS3	0.98	1.03	1.08	
		VOS2	1.08	1.13	1.18	
		VOS1	1.18	1.23	1.28	
		VOS0	1.33	1.38	1.40	

Table 12. General operating conditions (continued)

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
f_{CPU}	Arm® Cortex®-M7 clock frequency	VOS3	-	-	170	MHz
		VOS2	-	-	300	
		VOS1	-	-	400	
		VOS0	-	-	520	
		VOS0 and CPU_FREQ_BOOST	-	-	550	
f_{ACLK}	AXI clock frequency	VOS3	-	-	85	
		VOS2	-	-	150	
		VOS1	-	-	200	
		VOS0	-	-	275	
f_{HCLK}	AHB clock frequency	VOS3	-	-	85	
		VOS2	-	-	150	
		VOS1	-	-	200	
		VOS0	-	-	275	
f_{PCLK}	APB clock frequency	VOS3	-	-	42.5(5)	
		VOS2	-	-	75	
		VOS1	-	-	100	
		VOS0	-	-	137.5	
T_A(6)	Ambient temperature for temperature range 3	Maximum power dissipation	−40		125	°C
	Ambient temperature for temperature range 6	Maximum power dissipation	−40		85	
		Low-power dissipation(7)	−40		105	

1. When RESET is released, the functionality is guaranteed down to V_{PDRmax} or down to the specified V_{DDmin} when the PDR is OFF. The PDR can only be switched OFF though the PDR_ON pin that not available in all packages.
2. V_{BAT} minimum value can be reduced to 0 V if V_{DD} is present.
3. This formula has to be applied on power supplies related to the I/O structure described by the pin definition table.
4. At startup, the external V_{CORE} voltage must remain higher or equal to 1.10 V before disabling the internal regulator (LDO).
5. This value corresponds to the maximum APB clock frequency when at least one peripheral is enabled.
6. The device junction temperature must be kept below maximum T_J indicated in *Table 13: Supply voltage and maximum temperature configuration* and the maximum temperature.
7. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.6: Thermal characteristics*).

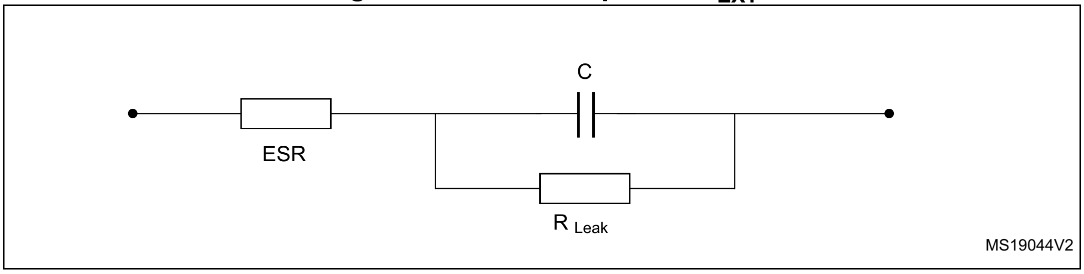
Table 13. Supply voltage and maximum temperature configuration

Power scale	V_{CORE} source	Max. T_J (°C)	Min. V_{DD}(V)	Min. V_{DDLDO} (V)
VOS0	LDO	105	1.7	1.7
	External (Bypass)		1.62	-
VOS1	LDO	125	1.62	1.62
	External (Bypass)		-	-
VOS2 or VOS3	LDO	125	1.62	1.62
	External (Bypass)		-	-
SVOS4/SVOS5	LDO	125	2	2
		105	1.62	1.62
	External (Bypass)	125	1.62	-

6.3.2 VCAP external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the VCAP pin. C_{EXT} is specified in *Table 14*. Two external capacitors can be connected to VCAP pins.

Figure 12. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 14. VCAP operating conditions(1)

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 µF(2)(3)
ESR	ESR of external capacitor	< 100 mΩ

1. When bypassing the voltage regulator, the two 2.2 µF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.
2. This value corresponds to CEXT typical value. A variation of +/-20% is tolerated.
3. If a third VCAP pin is available on the package, it must be connected to the other VCAP pins but no additional capacitor is required.

6.3.3 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 15. Operating conditions at power-up/power-down

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	10	∞	
t_{VDDA}	V_{DDA} rise time rate	0	∞	
	V_{DDA} fall time rate	10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	0	∞	
	V_{DDUSB} fall time rate	10	∞	
t_{VCORE}(1)	V_{CORE} rise time rate(2)	0	285	
	V_{CORE} fall time rate	10	∞	

1. t_{VCORE} should be achieved when V_{CORE} is provided by an external supply voltage (bypass with VDDLDO = V_{CORE}).
2. V_{CORE} rising slope must respect the above constraints. There are no constraints on the delay between V_{DD} rising and V_{CORE} rising.

6.3.4 Embedded reset and power control block characteristics

The parameters given in *Table 16* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 12: General operating conditions*.

Table 16. Reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$ (1)	Reset temporization after BOR0 released	-	-	377	550	µs
$V_{BOR0/POR/PDR}$	Power-on/power-down reset threshold	Rising edge(1)	1.62	1.67	1.71	V
		Falling edge	1.58	1.62	1.68	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.04	2.10	2.15	
		Falling edge	1.95	2.00	2.06	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.34	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.63	2.70	2.78	
		Falling edge	2.54	2.61	2.68	
V_{PVD0}	Programmable Voltage Detector threshold 0	Rising edge	1.90	1.96	2.01	
		Falling edge	1.81	1.86	1.91	
V_{PVD1}	Programmable Voltage Detector threshold 1	Rising edge	2.05	2.10	2.16	
		Falling edge	1.96	2.01	2.06	
V_{PVD2}	Programmable Voltage Detector threshold 2	Rising edge	2.19	2.26	2.32	
		Falling edge	2.10	2.15	2.21	
V_{PVD3}	Programmable Voltage Detector threshold 3	Rising edge	2.35	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{PVD4}	Programmable Voltage Detector threshold 4	Rising edge	2.49	2.56	2.62	
		Falling edge	2.39	2.45	2.51	
V_{PVD5}	Programmable Voltage Detector threshold 5	Rising edge	2.64	2.71	2.78	
		Falling edge	2.55	2.61	2.68	
V_{PVD6}	Programmable Voltage Detector threshold 6	Rising edge	2.78	2.86	2.94	
		Falling edge in Run mode	2.69	2.76	2.83	
$V_{hyst\_POR\_PDR}$	Hysteresis voltage for Power-on/power-down reset (including BOR0)	Hysteresis in Run mode	-	43.00	-	mV
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage for BOR (except BOR0)	Hysteresis in Run mode	-	100	-	
$I_{DD\_BOR\_PVD}$ (1)	BOR and PVD consumption from V_{DD}	-	-	-	0.630	µA
$I_{DD\_POR\_PVD}$	POR and PVD consumption from V_{DD}	-	0.8	-	1.200	

Table 16. Reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AVM_0}	Analog voltage detector for V_{DDA} threshold 0	Rising edge	1.66	1.71	1.76	V
		Falling edge	1.56	1.61	1.66	
V_{AVM_1}	Analog voltage detector for V_{DDA} threshold 1	Rising edge	2.06	2.12	2.19	
		Falling edge	1.96	2.02	2.08	
V_{AVM_2}	Analog voltage detector for V_{DDA} threshold 2	Rising edge	2.42	2.50	2.58	
		Falling edge	2.35	2.42	2.49	
V_{AVM_3}	Analog voltage detector for V_{DDA} threshold 3	Rising edge	2.74	2.83	2.91	
		Falling edge	2.64	2.72	2.80	
V_{hyst_VDDA}	Hysteresis of V_{DDA} voltage detector	-	-	100	-	mV
I_{DD_PVM}	PVM consumption from $V_{DD(1)}$	-	-	-	0.25	µA
I_{DD_VDDA}	Voltage detector consumption on V_{DDA}(1)	Resistor bridge	-	-	2.5	µA

1. Guaranteed by design.

6.3.5 Embedded reference voltage characteristics

The parameters given in *Table 17* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 12: General operating conditions*.

Table 17. Embedded reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltages	$-40°C < T_J < T_{Jmax}$	1.180	1.216	1.255	V
$t_{S\_vrefint}$(1)(2)(3)	ADC sampling time when reading the internal reference voltage	-	4.3	-	-	µs
t_{S_vbat}(2)	VBAT sampling time when reading the internal VBAT reference voltage	-	9	-	-	
$t_{start\_vrefint}$(2)	Start time of reference voltage buffer when ADC is enable	-	-	-	4.4	
I_{refbuf}(2)	Reference Buffer consumption for ADC	V_{DD} = 3.3 V	9	13.5	23	µA
ΔV_{REFINT}(2)	Internal reference voltage spread over the temperature range	$-40°C < T_J < T_{Jmax}$	-	5	15	mV
T_{coeff}(2)	Average temperature coefficient	Average temperature coefficient	-	20	70	ppm/°C
$V_{DDcoeff}$(2)	Average Voltage coefficient	$3.0 V < V_{DD} < 3.6 V$	-	10	1370	ppm/V

Table 17. Embedded reference voltage (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT_DIV1}	1/4 reference voltage	-	-	25	-	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage	-	-	50	-	
V_{REFINT_DIV3}	3/4 reference voltage	-	-	75	-	

1. The shortest sampling time for the application can be determined by multiple iterations.
2. Guaranteed by design.
3. Guaranteed by design. and tested in production at 3.3 V.

Table 18. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C, V_{DDA} = 3.3 V	1FF1 E860 - 1FF1 E861

6.3.6 Embedded USB regulator characteristics

The parameters given in *Table 19* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 12: General operating conditions*.

Table 19. USB regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REGOUTV33V}$	Regulated output voltage	-	3	-	3.6	V
I_{OUT}	Output current load sinked by USB block	-	-	-	20	mA
T_{WKUP}	Wakeup time	-	-	120	170	us

6.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 11: Current consumption measurement scheme*.

All the Run-mode current consumption measurements given in this section are performed with a CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The flash memory access time is adjusted with the minimum wait states number, depending on the f_{ACLK} frequency (refer to the table “Number of wait states according to CPU clock ($f_{rcc\_c\_ck}$) frequency and V_{CORE} range” available in the reference manual).
- When the peripherals are enabled, the AHB clock frequency is the CPU frequency divided by 2 and the APB clock frequency is AHB clock frequency divided by 2.
- For typical values, the power supply is 3 V unless otherwise specified.

The parameters given in the below tables are derived from tests performed at supply voltage conditions summarized in *Table 12: General operating conditions*, and at ambient temperature unless otherwise specified.

Table 20. Typical and maximum current consumption in Run mode, code with data processing running from ITCM(1)

Symbol	Parameter	Conditions		$f_{rcc\_c\_ck}$ (MHz)	Typ	Max(2) T_J = 25 °C	Max(2) T_J = 85 °C	Max(2) T_J = 105 °C	Max(2) T_J = 125 °C	Unit
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS0(3)	550	145	170	260	330	-	mA
				520	135	160	260	320	-	
			VOS0	520	135	160	260	320	-	
				480	125	150	250	310	-	
				450	115	150	240	300	-	
				400	105	130	230	290	-	
			VOS1	400	90.5	110	170	220	280	
				300	69.5	84	150	200	260	
			VOS2	300	63	74	130	170	220	
				280	58	69	120	160	210	
				216	45.5	56	110	150	200	
				200	42	53	110	140	200	
			VOS3	170	32.5	40	80	110	160	
				168	32	40	79	110	160	
				144	28	36	75	110	150	
				60	13.5	21	61	90	140	
				25	6.9	14	54	83	130	
		All peripherals enabled	VOS0(3)	550	215	250	360	430	-	
				520	205	240	350	420	-	
			VOS0	520	205	240	350	420	-	
				400	160	190	300	370	-	
			VOS1	400	135	160	230	290	360	
				300	105	130	200	250	330	
			VOS2	300	95	110	170	210	280	
				280	88	100	160	210	270	
			VOS3	170	49	58	110	140	190	

1. Data are in DTCM for best computation performance, the cache has no influence on consumption in this case.
2. Guaranteed by characterization results, unless otherwise specified.
3. CPU_FREQ_BOOST is enabled.

Table 21. Typical and maximum current consumption in Run mode, code with data processing running from flash memory, cache ON(1)

Symbol	Parameter	Conditions		$f_{rcc\_c\_ck}$ (MHz)	Typ	Max(2)				Unit
						T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS0(3)	550	145	170	270	330	-	mA
				520	140	170	260	320	-	
			VOS0	520	140	170	260	320	-	
				400	110	140	230	290	-	
			VOS1	400	92	110	180	220	290	
				300	71	86	150	200	260	
			VOS2	300	64	75	130	170	220	
				280	59	70	120	160	210	
				216	46.5	-	-	-	-	
				200	42.5	53	110	140	200	
				180	36	43	83	120	160	
			VOS3	170	33.5	41	81	110	160	
				168	33	-	-	-	-	
				144	29	-	-	-	-	
				60	14	-	-	-	-	
				25	6.85	-	-	-	-	
		All peripherals enabled	VOS0 (3)	550	220	250	360	430	-	
				520	210	240	350	420	-	
			VOS0	520	210	240	350	420	-	
				400	160	190	300	370	-	
			VOS1	400	140	160	240	290	360	
				300	105	130	200	250	330	
			VOS2	300	96	110	170	210	280	
				280	89	110	160	210	270	
			VOS3	170	50	59	110	140	190	

1. Data are in DTCM for best computation performance, the cache has no influence on consumption in this case.
2. Guaranteed by characterization results, unless otherwise specified.
3. CPU_FREQ_BOOST is enabled.

Table 22. Typical and maximum current consumption in Run mode, code with data processing running from flash memory, cache OFF(1)

Symbol	Parameter	Conditions		$f_{rcc\_c\_ck}$ (MHz)	Typ	Unit
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS0(2)	550	99	mA
				520	95	
			VOS0	520	95	
				400	76.5	
			VOS1	400	66.5	
				300	51.5	
			VOS2	300	47.5	
				280	43.5	
			VOS3	170	24.5	
		All peripherals enabled	VOS0(2)	550	170	
				520	165	
			VOS0	520	165	
				400	130	
			VOS1	400	115	
				300	87	
			VOS2	300	79	
				280	73.5	
			VOS3	170	41	

1. Data are in DTCM for best computation performance, the cache has no influence on consumption in this case.
2. CPU_FREQ_BOOST is enabled.

Table 23. Typical consumption in Run mode and corresponding performance versus code position

Symbol	Parameter	Conditions		$f_{rcc\_c\_ck}$ (MHz)	Coremark	Typ	Unit	I_{DD}/ Coremark	Unit
		Peripheral	Code						
I_{DD}	Supply current in Run mode	All peripherals disabled, cache ON	ITCM	550	2777	145	mA	52.2	µA/ Core-mark
			FLASH	550	2777	145		52.2	
			AXI SRAM	550	2777	145		52.2	
			SRAM 1	550	2777	150		54.0	
			SRAM 4	550	2777	145		52.2	
		All peripherals disabled cache OFF	FLASH	550	923	99		107.3	
			AXI SRAM	550	1271	105		82.6	
			SRAM 1	550	790	96.5		122.2	
			SRAM 4	550	723	89.5		123.8	

Table 24. Typical current consumption in Autonomous mode

Symbol	Parameter	Conditions		$f_{rcc\_c\_ck}$ (MHz)	Typ	Unit
I_{DD}	Supply current in Autonous mode	Run, D1Stop, D2Stop	VOS3	64	3.6	mA
		Run, D1Standby, D2Standby	VOS3	64	2.6	

Table 25. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions		$f_{rcc\_c\_ck}$ (MHz)	Typ	Max(1)				Unit
						T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
$I_{DD(Sleep)}$	Supply current in Sleep mode	All peripherals disabled	VOS0 (2)	550	36	-	-	-	-	mA
				520	33.5	60	170	240	-	
			VOS0	520	33.5	60	170	240	-	
				400	27	52	160	230	-	
			VOS1	400	22.5	39	110	170	240	
				300	18.5	34	110	160	240	
			VOS2	300	16.5	28	85	130	190	
				170	9.7	21	78	120	190	
			VOS3	170	8.5	17	61	96	150	

1. Guaranteed by characterization results.
2. CPU_FREQ_BOOST is enabled.

Table 26. Typical and maximum current consumption in Stop mode

Symbol	Parameter	Conditions		Typ	Max(1)				Unit
					T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
$I_{DD(Stop)}$	Supply current in Stop and DStop modes	Flash memory in low-power mode	SVOS5	0.52	3.7	26	44	72	mA
			SVOS4	0.81	6.1	39	64	110	
			SVOS3	1.15	8.6	51	82	130	
		Flash memory in normal mode	SVOS5	0.535	3.7	26	44	72	
			SVOS4	0.96	6.2	39	64	110	
			SVOS3	1.45	8.8	51	83	130	

1. Guaranteed by characterization results.

Table 27. Typical and maximum current consumption in Standby mode

Symbol	Parameter	Conditions		Typ(1)				Max at 3.6 V(2)				Unit
		Backup SRAM	RTC and LSE(3)	1.65 V	2.4 V	3 V	3.3 V	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DD} (Standby)	Supply current in Standby mode, **IWDG OFF**	OFF	OFF	2.2	2.35	2.5	2.8	-	-	-	-	µA
		ON	OFF	3.5	3.7	4	4.3	-	-	-	-	
		OFF	ON	2.2	2.4	2.85	3.25	4.5	15	30	64	
		ON	ON	3.5	3.8	4.35	4.75	8.3	39	75	140	

1. These values are given for PDR OFF. When the PDR is ON, the typical current consumption is increased (refer to *Table 16: Reset and power control block characteristics*.
2. Guaranteed by characterization results.
3. The LSE is in Low-drive mode.

Table 28. Typical and maximum current consumption in V_{BAT} mode

Sym-bol	Para-meter	Conditions		Typ				Max at 3.6 V(1)(2)				Unit
		Back-up SRAM	RTC and LSE(3)	1.2 V	2 V	3 V	3.3 V	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DD} (VBAT)	Supply current in VBAT mode	OFF	OFF	0.008	0.01	0.025	0.05	0.3	3.1	7.4	18	µA
		ON	OFF	1.5	1.7	1.9	1.9	4	28	53	91	
		OFF	ON	0.4	0.5	0.75	0.8	-	-	-	-	
		ON	ON	1.8	2.1	2.8	3.2	-	-	-	-	

1. Guaranteed by characterization results.
2. The LDO regulator is used before switching to V_{BAT} mode.
3. The LSE is in Low-drive mode.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as input with pull-up or pull-down generate a current consumption when the pin is externally held to the opposite level.

The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 51: I/O static characteristics*.

For the output pins, any internal or external pull-up or pull-down and external load must also be considered to estimate the current consumption.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 29: Peripheral current consumption in Run mode*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal and external) connected to the pin:

$$I_{SW} = V_{DDx} \times f_{SW} \times C_L$$

where

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
- V_{DDx} is the MCU supply voltage
- f_{SW} is the I/O switching frequency
- C_L is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The I/O compensation cell is enabled.
- $f_{rcc\_c\_ck}$ is the CPU clock. $f_{PCLK} = f_{rcc\_c\_ck}/4$, and $f_{HCLK} = f_{rcc\_c\_ck}/2$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - $f_{rcc\_c\_ck}$ = 550 MHz (Scale 0), $f_{rcc\_c\_ck}$ = 400 MHz (Scale 1), $f_{rcc\_c\_ck}$ = 300 MHz (Scale 2), $f_{rcc\_c\_ck}$ = 170 MHz (Scale 3)
- The ambient operating temperature is 25 °C and V_{DD}=3.3 V
- The LDO regulator supplies V_{CORE}.

Table 29. Peripheral current consumption in Run mode

Peripheral		$I_{DD(Typ)}$				Unit
		VOS0	VOS1	VOS2	VOS3	
AHB3	MDMA	3.70	3.10	2.90	2.60	µA/MHz
	DMA2D	2.70	2.30	2.10	1.90	
	Flash memory	15.20	14.00	12.00	10.90	
	FMC registers	0.90	0.90	0.80	0.70	
	FMC kernel	7.00	6.10	5.60	5.40	
	OCTOSPI1 registers	1.40	1.30	0.50	0.40	
	OCTOSPI1 kernel	3.10	1.20	0.50	0.20	
	SDMMC1 registers	8.70	7.60	6.90	6.10	
	SDMMC1 kernel	2.10	1.80	1.40	1.20	
	OCTOSPI2 registers	1.40	1.30	0.90	0.60	
	OCTOSPI2 kernel	2.50	1.50	1.40	0.50	
	OTFDEC1	0.80	0.70	0.10	0.10	
	OTFDEC2	0.80	0.70	0.10	0.10	
	AXI SRAM	8.50	7.50	6.90	6.00	

Table 29. Peripheral current consumption in Run mode (continued)

Peripheral		$I_{DD(Typ)}$				Unit
		VOS0	VOS1	VOS2	VOS3	
AHB1	DMA1	0.70	0.60	0.50	0.40	µA/MHz
	DMA2	1.00	0.80	0.70	0.70	
	DMAMUX1	0.10	0.10	0.10	0.10	
	ADC1/2 registers	4.50	4.00	3.60	2.30	
	ADC1/2 kernel	0.90	0.80	0.60	0.40	
	USB1 registers	20.80	17.50	16.50	14.80	
	USB1 kernel	1.20	0.90	0.90	0.90	
	USB1 ULPI kernel	31.00	30.00	29.50	27.00	
	Ethernet	17.30	14.40	13.70	12.30	
AHB2	DCMI	4.80	4.00	3.80	3.40	µA/MHz
	CRYP	1.40	1.20	1.10	0.80	
	HASH1	1.70	1.40	1.30	1.00	
	HSEM	0.60	0.60	0.10	0.10	
	RNG1 registers	1.20	1.00	0.90	0.70	
	RNG1 kernel	15.00	13.60	10.00	9.00	
	SDMMC2 registers	15.00	12.20	11.70	10.40	
	SDMMC2 kernel	2.10	1.80	1.40	1.20	
	BDMA	6.50	5.90	4.80	4.30	
	SRAM1	2.40	2.00	1.80	1.60	
	SRAM2	2.70	2.30	2.00	1.80	
	CORDIC	0.80	0.60	0.50	0.50	
	FMAC	2.40	2.10	1.90	1.60	

Table 29. Peripheral current consumption in Run mode (continued)

Peripheral		$I_{DD(Typ)}$				Unit
		VOS0	VOS1	VOS2	VOS3	
AHB4	GPIOA	0.10	0.10	0.10	0.10	µA/MHz
	GPIOB	0.90	0.80	0.10	0.10	
	GPIOC	0.50	0.10	0.10	0.10	
	GPIOD	0.90	0.80	0.10	0.10	
	GPIOE	0.90	0.80	0.10	0.10	
	GPIOF	0.30	0.10	0.10	0.10	
	GPIOG	0.90	0.80	0.30	0.20	
	GPIOH	0.10	0.10	0.10	0.10	
	GPIOJ	0.90	0.80	0.30	0.20	
	GPIOK	0.80	0.80	0.10	0.10	
	HSEM	0.60	0.60	0.10	0.10	
	BDMA	6.50	5.90	4.80	4.30	
	CRC	0.90	0.30	0.30	0.30	
	ADC3 registers	2.10	1.40	1.30	1.20	
	ADC3 kernel	0.40	0.30	0.30	0.20	
	Backup SRAM	1.80	1.00	1.00	0.80	
APB3	LTDC	9.00	7.90	7.70	6.40	
	WWDG1	0.60	0.50	0.50	0.50	

Table 29. Peripheral current consumption in Run mode (continued)

Peripheral		$I_{DD(Typ)}$				Unit
		VOS0	VOS1	VOS2	VOS3	
APB1	TIM2	4.50	4.40	3.30	3.00	µA/MHz
	TIM3	3.80	3.20	2.90	2.70	
	TIM4	3.60	3.10	2.60	2.50	
	TIM5	4.10	3.40	3.10	2.90	
	TIM6	1.50	1.10	1.00	1.00	
	TIM7	1.40	1.10	0.90	0.90	
	TIM12	2.30	1.80	1.60	1.60	
	TIM13	1.90	1.40	1.30	1.20	
	TIM14	1.60	1.20	1.10	1.10	
	TIM23	4.60	3.90	3.60	3.40	
	TIM24	4.40	3.80	3.50	3.30	
	LPTIM1 registers	3.50	2.90	2.70	2.60	
	LPTIM1 kernel	2.60	2.30	2.00	1.80	
	SPI2 registers	2.10	1.60	0.90	0.80	
	SPI2 kernel	1.50	1.20	1.10	1.00	
	SPI3 registers	2.40	2.00	1.90	1.80	
	SPDIFRX registers	0.60	0.50	0.50	0.50	
	SPDIFRX kernel	3.50	2.80	2.40	2.20	
	USART2 registers	6.60	5.70	5.20	4.90	
	USART2 kernel	4.80	4.80	4.60	3.80	
	USART3 registers	5.90	5.40	4.60	4.30	
	USART3 kernel	4.00	3.40	3.00	2.90	
	UART4 registers	5.60	4.80	3.50	3.10	
	UART4 kernel	3.80	3.20	3.00	2.40	
	UART5 registers	5.60	4.60	4.40	4.00	
	UART5 kernel	3.90	3.40	3.30	3.20	
	UART7 registers	5.40	4.60	4.20	3.90	
	UART7 kernel	3.80	3.30	3.00	3.00	
	UART8 registers	5.60	4.10	3.50	3.40	
	UART8 kernel	3.60	3.20	3.20	3.10	
	I2C1 registers	0.90	0.60	0.60	0.50	
	I2C1 kernel	2.30	2.00	1.80	1.60	
	I2C2 registers	1.00	0.70	0.60	0.60	

Table 29. Peripheral current consumption in Run mode (continued)

Peripheral		$I_{DD(Typ)}$				Unit
		VOS0	VOS1	VOS2	VOS3	
APB1	I2C2 kernel	2.30	1.90	1.70	1.20	µA/MHz
	I2C3 registers	0.90	0.60	0.50	0.50	
	I2C3 kernel	2.30	2.00	1.00	1.00	
	I2C5 registers	0.90	0.60	0.50	0.50	
	I2C5 kernel	2.20	2.10	1.90	1.80	
	CEC registers	0.60	0.30	0.20	0.20	
	CEC kernel	0.10	0.10	0.10	0.10	
	DAC1	1.60	1.30	1.10	1.10	
	FDCAN1/2/3 registers	24.10	20.90	18.20	17.40	
	FDCAN1/2/3 kernel	9.90	9.90	9.00	8.00	
	CRS	4.90	3.90	3.50	3.20	
	SWPMI registers	1.10	0.80	0.80	0.80	
	SWPMI kernel	1.50	1.10	1.00	1.00	
	OPAMP	0.50	0.40	0.30	0.20	

Table 29. Peripheral current consumption in Run mode (continued)

Peripheral		$I_{DD(Typ)}$				Unit
		VOS0	VOS1	VOS2	VOS3	
APB2	TIM1	5.30	4.40	4.20	3.80	µA/MHz
	TIM8	5.60	5.40	5.20	3.90	
	USART1 registers	1.80	1.60	1.40	1.10	
	USART1 kernel	3.00	2.90	2.80	2.70	
	USART6 registers	1.90	1.70	1.50	1.20	
	USART6 kernel	4.50	4.00	3.60	3.10	
	UART9 registers	1.70	1.70	1.60	1.10	
	UART9 kernel	3.80	3.30	2.90	2.90	
	USART10 registers	1.80	1.70	1.40	1.10	
	USART10 kernel	3.80	3.30	2.90	2.90	
	SPI1 registers	1.90	1.80	1.40	1.20	
	SPI1 kernel	1.50	1.20	1.10	1.00	
	SPI4 registers	1.80	1.60	1.40	1.10	
	SPI4 kernel	1.50	1.20	1.10	1.00	
	SPI5 registers	1.60	1.60	1.40	1.10	
	SPI5 kernel	1.50	1.20	1.10	1.00	
	TIM15	2.80	2.50	2.30	1.90	
	TIM16	2.00	1.90	1.60	1.30	
	TIM17	2.10	2.00	1.70	1.40	
	SAI1 registers	1.40	1.40	1.20	0.90	
	SAI1 kernel	0.80	0.70	0.70	0.70	
	DFSDM1 registers	5.60	5.40	5.30	4.00	
	DFSDM1 kernel	0.30	0.20	0.20	0.10	
	SYSCFG	1.20	1.10	1.10	1.10	

Table 29. Peripheral current consumption in Run mode (continued)

Peripheral		$I_{DD(Typ)}$ VOS0	VOS1	VOS2	VOS3	Unit
APB4	LPUART1 registers	1.80	0.90	0.80	0.60	µA/MHz
	LPUART1 kernel	2.40	2.30	2.00	1.90	
	SPI6 registers	2.60	2.30	2.10	1.80	
	SPI6 kernel	1.20	1.10	1.00	0.90	
	I2C4 registers	0.70	0.70	0.60	0.40	
	I2C4 kernel	2.00	1.70	1.70	1.40	
	LPTIM2 registers	1.50	0.70	0.50	0.30	
	LPTIM2 kernel	2.50	2.10	2.00	1.90	
	LPTIM3 registers	2.90	2.60	2.30	1.90	
	LPTIM3 kernel	2.40	2.00	1.90	1.70	
	LPTIM4 registers	2.60	2.30	2.10	1.80	
	LPTIM4 kernel	2.10	1.80	1.70	1.60	
	LPTIM5 registers	2.60	2.30	2.00	1.70	
	LPTIM5 kernel	2.10	1.80	1.60	1.50	
	COMP1/2	0.70	0.30	0.20	0.10	
	VREF	0.10	0.10	0.10	0.10	
	RTC	0.10	0.10	0.10	0.10	
	WWDG1	0.60	0.50	0.50	0.50	
	SAI4 registers	2.40	2.20	2.10	1.70	
	SAI4 kernel	0.90	0.90	0.90	0.70	
	DTS	2.90	2.60	2.30	2.00	

6.3.8 Wake-up time from low-power modes

The wake-up times given in *Table 30* are measured starting from the wake-up event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wake-up event is WFE.
- WKUP (PC1) pin is used to wake-up from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Table 30. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ(1)	Max(1)(2)	Unit
$t_{WUSLEEP}$(3)	Wakeup from Sleep	-	14.00	15.00	CPU clock cycles
t_{WUSTOP}(3)	Wakeup from Stop mode	SVOS3, HSI, flash memory in Normal mode	4.6	6.2	µs
		SVOS3, HSI, flash memory in low-power mode	12.4	17.4	
		SVOS4, HSI, flash memory in Normal mode	15.5	21.1	
		SVOS4, HSI, flash memory in low-power mode	23.3	31.8	
		SVOS5, HSI, flash memory in Normal mode	39.1	52.6	
		SVOS5, HSI, flash memory in low-power mode	39.1	52.7	
		SVOS3, CSI, flash memory in Normal mode	30.0	41.6	
		SVOS3, CSI, flash memory in low-power mode	40.6	55.0	
		SVOS4, CSI, flash memory in Normal mode	41.0	55.4	
		SVOS4, CSI, flash memory in low-power mode	51.5	68.8	
		SVOS5, CSI, flash memory in Normal mode	67.3	89.5	
		SVOS5, CSI, flash memory in low-power mode	67.2	89.5	
$t_{WUSTDBY}$(3)	Wakeup from Standby mode	-	400.0	504.3	

1. Guaranteed by characterization results.
2. The maximum values have been measured at -40 °C, in worst conditions.
3. The wake-up times are measured from the wake-up event to the point in which the application code reads the first

6.3.9 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O.

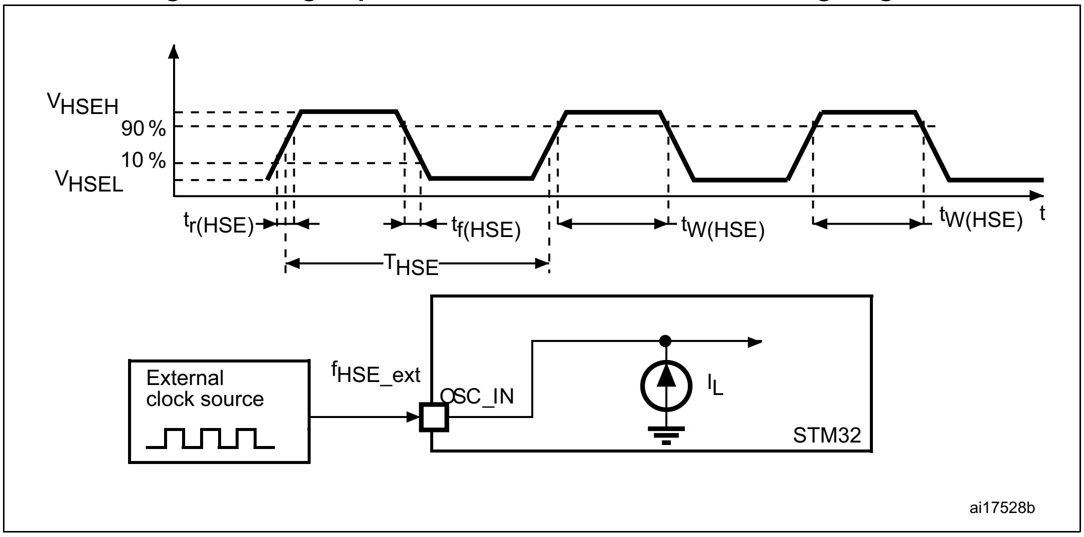
The external clock signal has to respect the *Table 51: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 13*.

Table 31. High-speed external user clock characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	4	25	50	MHz
V_{HSEH}	Digital OSC_IN input high-level voltage	0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	Digital OSC_IN input low-level voltage	V_{SS}	-	0.3 V_{DD}	
$t_{W(HSE)}$	OSC_IN high or low time	7	-	-	ns

1. Guaranteed by design.

Figure 13. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

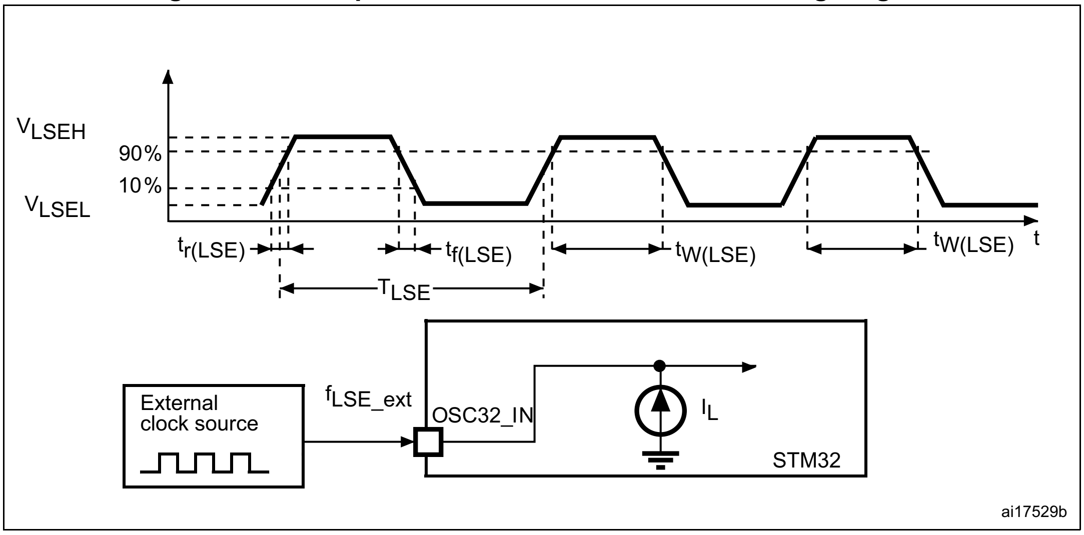
In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 51: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 14*.

Table 32. Low-speed external user clock characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high-level voltage	-	0.7 V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low-level voltage	-	V_{SS}	-	0.3 V_{DD}	V
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Figure 14. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 50 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 33*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

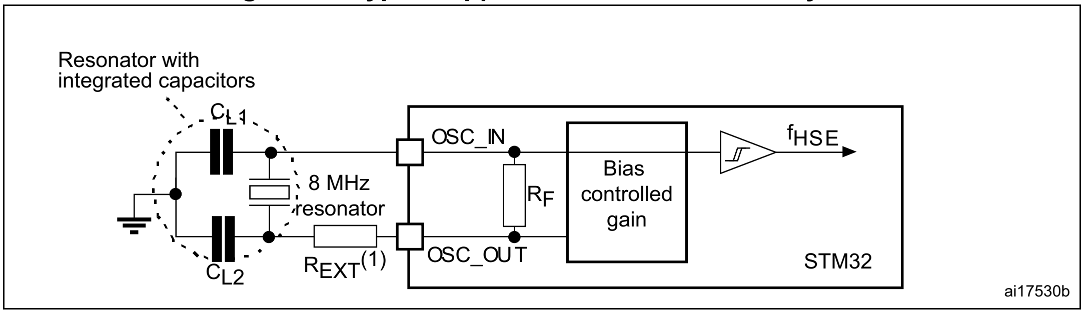
Table 33. 4-50 MHz HSE oscillator characteristics(1)

Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	4	-	50	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	4	mA
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 4 MHz	-	0.35	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 8 MHz	-	0.40	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 16 MHz	-	0.45	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 32 MHz	-	0.65	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 48 MHz	-	0.95	-	
$Gm_{critmax}$	Maximum critical crystal gm	Startup	-	-	1.5	mA/V
t_{SU}(4)	Start-up time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to application note AN2867 “Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs” available from the ST website www.st.com.

Figure 15. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 34*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

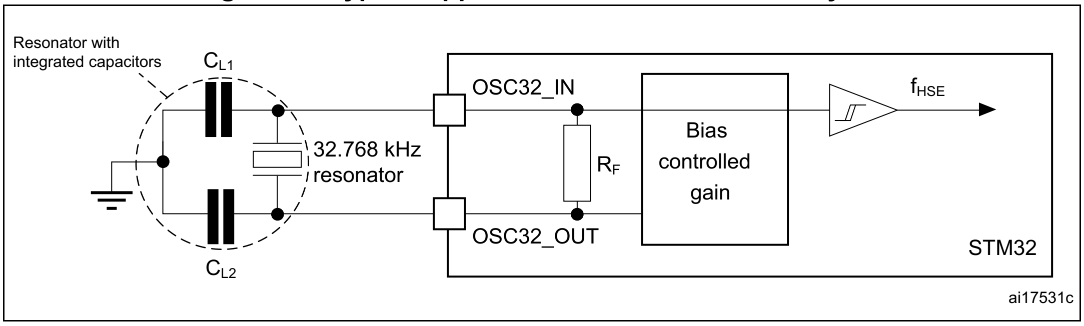
Table 34. Low-speed external user clock characteristics(1)

Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	-	32.768	-	kHz
I_{DD}	LSE current consumption	LSEDRV[1:0] = 00, Low drive capability	-	290	-	nA
		LSEDRV[1:0] = 01, Medium Low drive capability	-	390	-	
		LSEDRV[1:0] = 10, Medium high drive capability	-	550	-	
		LSEDRV[1:0] = 11, High drive capability	-	900	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00, Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01, Medium Low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10, Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, High drive capability	-	-	2.7	
t_{SU}(3)	Startup time	VDD is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 *“Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs”*.
3. t_{SU} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768k Hz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs" available from the ST website www.st.com.

Figure 16. Typical application with a 32.768 kHz crystal



1. *An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.*

6.3.10 Internal clock source characteristics

The parameters given in Table 35 to Table 37 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 12: General operating conditions.

48 MHz high-speed internal RC oscillator (HSI48)

Table 35. HSI48 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 frequency	V_{DD}=3.3 V, TJ=30 °C	47.5(1)	48	48.5(1)	MHz
TRIM(2)	USER trimming step	-	-	0.175	0.250	%
USER TRIM COVERAGE(3)	USER TRIMMING coverage	± 32 steps	±4.70	±5.6	-	%
DuCy(HSI48)(2)	Duty Cycle	-	45	-	55	%
ACCHSI48_REL(3)(4)	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	T_J=-40 to 125 °C	–4.5	-	3.5	%
Δ_{VDD}(HSI48)(2)(5)	HSI48 oscillator frequency drift with V_{DD}(6) (the reference is 3.3 V)	V_{DD}=3 to 3.6 V	-	0.025	0.05	%
		V_{DD}=1.62 V to 3.6 V	-	0.05	0.1	
$t_{su(HSI48)}$(2)	HSI48 oscillator start-up time	-	-	2.1	4.0	μs
$I_{DD(HSI48)}$(2)	HSI48 oscillator power consumption	-	-	350	400	μA
N_T jitter(2)	Next transition jitter Accumulated jitter on 28 cycles(7)	-	-	± 0.15	-	ns
P_T jitter(2)	Paired transition jitter Accumulated jitter on 56 cycles(7)	-	-	± 0.25	-	ns

1. Guaranteed by test in production.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. $\Delta f_{HSI} = ACCHSI48\_REL + \Delta_{VDD}$.

5. Δf_{HSI} = ACCHSI48_REL + Δ_{VDD}.
6. These values are obtained by using the formula: (Freq(3.6 V) - Freq(3.0 V)) / Freq(3.0 V) or (Freq(3.6 V) - Freq(1.62 V)) / Freq(1.62 V).
7. Jitter measurements are performed without clock source activated in parallel.

64 MHz high-speed internal RC oscillator (HSI)

Table 36. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI frequency	V_{DD}=3.3 V, T_J=30 °C	63.7(2)	64	64.3(2)	MHz
TRIM	HSI user trimming step	Trimming is not a multiple of 32	-	0.24	0.32	%
		Trimming is 128, 256 and 384	−5.2	−1.8	-	
		Trimming is 64, 192, 320 and 448	−1.4	−0.8	-	
		Other trimming are a multiple of 32 (not including multiple of 64 and 128)	−0.6	−0.25	-	
DuCy(HSI)	Duty cycle	-	45	-	55	%
$\Delta_{VDD\ (HSI)}$	HSI oscillator frequency drift over V_{DD} (the reference is 3.3 V)	V_{DD}=1.62 to 3.6 V	−0.12	-	0.03	%
$\Delta_{TEMP(HSI)}$	HSI oscillator frequency drift over temperature (the reference is 64 MHz)	T_J=-20 to 105 °C	−1(3)	-	1(3)	%
		T_J=−40 to $T_J$max °C	−2(3)	-	1(3)	
t_{su}(HSI)	HSI oscillator start-up time	-	-	1.4	2	µs
t_{stab}(HSI)	HSI oscillator stabilization time	at 1% of target frequency	-	4	8	
		at 5% of target frequency	-	-	4	
I_{DD}(HSI)	HSI oscillator power consumption	-	-	300	400	µA

1. Guaranteed by design unless otherwise specified.
2. Guaranteed by test in production.
3. Guaranteed by characterization results.

4 MHz low-power internal RC oscillator (CSI)

Table 37. CSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CSI}	CSI frequency	V_{DD}=3.3 V, T_J=30 °C	3.96(2)	4	4.04(2)	MHz
TRIM	CSI trimming step	Trimming is not a multiple of 16	-	0.40	0.75	%
		Trimming is a multiple of 32	−4.75	−2.75	0.75	
		Other trimming values not multiple of 16 (excluding multiple of 32)	−0.43	0.00	0.75	
DuCy(CSI)	Duty cycle	-	45	-	55	%
Δ_{TEMP} (CSI)	CSI oscillator frequency drift over temperature	T_J = 0 to 85 °C	−3.7(3)	-	4.5(3)	%
		T_J = −40 to 125 °C	−11(3)	-	7.5(3)	
Δ_{VDD} (CSI)	CSI oscillator frequency drift over V_{DD}	V_{DD} = 1.62 to 3.6 V	−0.06	-	0.06	%
$t_{su(CSI)}$	CSI oscillator startup time	-	-	1	2	µs
$t_{stab(CSI)}$	CSI oscillator stabilization time (to reach ± 3% of f_{CSI})	-	-	-	4	cycle
$I_{DD(CSI)}$	CSI oscillator power consumption	-	-	23	30	µA

1. Guaranteed by design, unless otherwise specified.
2. Guaranteed by test in production.
3. Guaranteed by characterization results.

Low-speed internal (LSI) RC oscillator

Table 38. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	V_{DD} = 3.3 V, T_J = 25 °C	31.4(1)	32	32.6(1)	kHz
		T_J = –40 to 110 °C, V_{DD} = 1.62 to 3.6 V	29.76(2)	-	33.6(2)	
		T_J = –40 to 125 °C, V_{DD} = 1.62 to 3.6 V	29.4(2)	-	33.6(2)	
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	80	130	µs
$t_{stab(LSI)}$(3)	LSI oscillator stabilization time (5% of final value)	-	-	120	170	
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	-	130	280	nA

1. Guaranteed by test in production.
2. Guaranteed by characterization results.
3. Guaranteed by design.

6.3.11 PLL characteristics

The parameters given in *Table 39*, *Table 42* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 12: General operating conditions*.

Table 39. PLL1 characteristics (wide VCO frequency range)(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-		2	-	16	MHz
	PLL input clock duty cycle	-		10	-	90	%
$f_{PLL\_P\_OUT}$	PLL multiplier output clock P	VOS0		1.5	-	550(2)	MHz
		VOS1		1.5	-	400(2)	
		VOS2		1.5	-	300(2)	
		VOS3		1.5	-	170(2)	
f_{VCO_OUT}	PLL VCO output	-		192	-	836(3)	
t_{LOCK}	PLL lock time	Normal mode		15	50	150(3)	µs
		Sigma-delta mode (CKIN ≥ 8 MHz)		25	65	170	
Jitter	Cycle-to-cycle jitter(4)	$f_{PLL\_OUT} = f_{VCO\_OUT}/100$	f_{VCO_OUT} = 192 MHz	-	51	-	ps
			f_{VCO_OUT} = 400 MHz	-	19	-	
			f_{VCO_OUT} = 560 MHz	-	10	-	
			f_{VCO_OUT} = 800 MHz	-	9	-	
	Period jitter		f_{VCO_OUT} = 192 MHz	-	38	-	
			f_{VCO_OUT} = 560 MHz	-	8	-	
			f_{VCO_OUT} = 800 MHz	-	7	-	
	Long term jitter	Normal mode (CKIN = 2 MHz)	f_{VCO_OUT} = 192 MHz	-	0.15	-	%
			f_{VCO_OUT} = 400 MHz	-	0.14	-	
			f_{VCO_OUT} = 832 MHz	-	0.16	-	
		Sigma-delta mode (CKIN = 16 MHz)	f_{VCO_OUT} = 192 MHz	-	0.17	-	
			f_{VCO_OUT} = 500 MHz	-	0.08	-	
			f_{VCO_OUT} = 836 MHz	-	0.06	-	

Table 39. PLL1 characteristics (wide VCO frequency range)[(1)] (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DD(PLL)}$	PLL power consumption	f_{VCO_OUT} = 560 MHz	V_{DDA}	530	557	670	µA
			V_{CORE}	1190	1285	6300	
		f_{VCO_OUT} = 192 MHz	V_{DDA}	260	286	513	
			V_{CORE}	309	377	5700	

1. Guaranteed by design unless otherwise specified.
2. This value must be limited to the maximum frequency due to the product limitation.
3. Guaranteed by characterization results.
4. Integer mode only.

Table 40. PLL1 characteristics (medium VCO frequency range)[(1)]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-		1	-	2	MHz
	PLL input clock duty cycle	-		10	-	90	%
f_{PLL_OUT}	PLL multiplier output clock P, Q, R	VOS0		1.17	-	210	MHz
		VOS1		1.17	-	210	
		VOS2		1.17	-	210	
		VOS3		1.17	-	200	
f_{VCO_OUT}	PLL VCO output	-		150	-	420	
t_{LOCK}	PLL lock time	Normal mode		-	60[(2)]	100[(2)]	µs
		Sigma-delta mode		forbidden			
Jitter	Cycle-to-cycle jitter[(3)]	-	f_{VCO_OUT} = 150 MHz	-	145	-	±ps
			f_{VCO_OUT} = 300 MHz	-	91	-	
			f_{VCO_OUT} = 400 MHz	-	64	-	
			f_{VCO_OUT} = 420 MHz	-	63	-	
	Period jitter	f_{PLL_OUT} = 50 MHz	f_{VCO_OUT} = 150 MHz	-	55	-	±-ps
			f_{VCO_OUT} = 400 MHz	-	30	-	
	Long term jitter	Normal mode	f_{VCO_OUT} = 400 MHz	-	±0.3	-	%
I(PLL)	PLL power consumption on V_{DD}	f_{VCO_OUT} = 420 MHz	VDD	-	440	1150	µA
			VCORE	-	530	-	
		f_{VCO_OUT} = 150 MHz	VDD	-	180	500	
			VCORE	-	200	-	

1. Guaranteed by design unless otherwise specified.
2. Guaranteed by characterization results.
3. Integer mode only.

Table 41. PLL2 and PLL3 characteristics (wide VCO frequency range)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-	2	-	16	MHz
	PLL input clock duty cycle	-	10	-	90	%
f_{PLL_OUT}	PLL multiplier output clock P, Q, R	VOS0	1.5	-	550(2)	MHz
		VOS1	1.5	-	400(2)	
		VOS2	1.5	-	300(2)	
		VOS3	1.5	-	170(2)	
f_{VCO_OUT}	PLL VCO output	-	192	-	960(3)	
t_{LOCK}	PLL lock time	Normal mode	-	50	150(3)	µs
		Sigma-delta mode (f_{PLL_IN} ≥ 8 MHz)	-	58	166(3)	
Jitter	Cycle-to-cycle jitter(4)	f_{VCO_OUT} = 192 MHz	-	134	-	±ps
		f_{VCO_OUT} = 200 MHz	-	134	-	
		f_{VCO_OUT} = 400 MHz	-	76	-	
		f_{VCO_OUT} = 800 MHz	-	39	-	
	Long term jitter	Normal mode (f_{PLL_IN} = 2 MHz), f_{VCO_OUT} = 560 MHz	-	±0.2	-	%
		Normal mode (f_{PLL_IN} = 16 MHz), f_{VCO_OUT} = 560 MHz	-	±0.8	-	
		Sigma-delta mode (f_{PLL_IN} = 2 MHz), f_{VCO_OUT} = 560 MHz	-	±0.2	-	
		Sigma-delta mode (f_{PLL_IN} = 16 MHz), f_{VCO_OUT} = 560 MHz	-	±0.8	-	
$I_{DD(PLL)}$(3)	PLL power consumption	f_{VCO_OUT} = 836 MHz, V_{DD}	-	590	1500	µA
		f_{VCO_OUT} = 836 MHz, V_{CORE}	-	720	-	
		f_{VCO_OUT} = 192 MHz, V_{DD}	-	180	600	
		f_{VCO_OUT} = 192 MHz, V_{CORE}	-	280	-	

1. Guaranteed by design unless otherwise specified.
2. This value must be limited to the maximum frequency due to the product limitation.

3. Guaranteed by characterization results.
4. Integer mode only.

Table 42. PLL2 and PLL3 characteristics (medium VCO frequency range)(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-		1	-	2	MHz
	PLL input clock duty cycle	-		10	-	90	%
f_{PLL_OUT}	PLL multiplier output clock P, Q, R	VOS0		1.17	-	210	MHz
		VOS1		1.17	-	210	-
		VOS2		1.17	-	210	-
		VOS3		1.17	-	200	-
f_{VCO_OUT}	PLL VCO output	-		150	-	420	-
t_{LOCK}	PLL lock time	Normal mode		-	60	100(2)	µs
		Sigma-delta mode		forbidden			
Jitter	Cycle-to-cycle jitter(3)	f_{VCO_OUT} = 150 MHz		-	145	-	±ps
		f_{VCO_OUT} = 200 MHz		-	91	-	
		f_{VCO_OUT} = 400 MHz		-	64	-	
		f_{VCO_OUT} = 420 MHz		-	63	-	
	Period jitter	f_{PLL_OUT} = 50 MHz	f_{VCO_OUT} = 150 MHz	-	55	-	±ps
		f_{VCO_OUT} = 400 MHz		-	30	-	
	Long term jitter	Normal mode	f_{VCO_OUT} = 400 MHz	-	±0.3	-	%
$I_{DD(PLL)}$	PLL power consumption on V_{DD}	f_{VCO_OUT} = 420 MHz	V_{DD}	-	440	1150	µA
			V_{CORE}	-	530	-	
		f_{VCO_OUT} = 150 MHz	V_{DD}	-	180	500	
			V_{CORE}	-	200	-	

1. Guaranteed by design unless otherwise specified.
2. Guaranteed by characterization results.
3. Integer mode only.

6.3.12 Memory characteristics

Flash memory

The characteristics are given at T_J = –40 to 125 °C unless otherwise specified.

The devices are shipped to customers with the flash memory erased.

Table 43. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode	-	6.5	-	mA
		Write / Erase 16-bit mode	-	11.5	-	
		Write / Erase 32-bit mode	-	20	-	
		Write / Erase 64-bit mode	-	35	-	

Table 44. Flash memory programming

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word (266 bits) programming time	Program/erase parallelism x 8	-	290	580(2)	µs
		Program/erase parallelism x 16	-	180	360	
		Program/erase parallelism x 32	-	130	260	
		Program/erase parallelism x 64	-	100	200	
t_{ERASE}	Sector (128 Kbytes) erase time	Program/erase parallelism x 8	-	2	4	s
		Program/erase parallelism x 16	-	1.8	3.6	
		Program/erase parallelism x 32	-	1.1	2.2	
t_{ME}	Mass erase time (1 Mbyte)	Program/erase parallelism x 8	-	13	26	
		Program/erase parallelism x 16	-	8	16	
		Program/erase parallelism x 32	-	6	12	
		Program/erase parallelism x 64	-	5	10	
V_{prog}	Programming voltage	Program parallelism x 8	1.62	-	3.6	V
		Program parallelism x 16				
		Program parallelism x 32				
		Program parallelism x 64	1.8	-	3.6	

1. Guaranteed by characterization results.
2. The maximum programming time is measured after 10K erase operations.

Table 45. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_J = –40 to +125 °C	10	kcycles
t_{RET}	Data retention	1 kcycle at T_A = 85 °C	30	Years
		10 kcycles at T_A = 55 °C	20	

1. Guaranteed by characterization results.

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 46*. They are based on the EMS levels and classes defined in application note AN1709 "*EMC design guide for STM8, STM32 and Legacy MCUs* ".

Table 46. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C, LQFP176, conforming to IEC 61000-4-2	3B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C, LQFP176, conforming to IEC 61000-4-4	5A

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore, it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015 *"Software techniques for improving microcontrollers EMC performance").*

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard, which specifies the test board and the pin loading.

Table 47. EMI characteristics for f_{HSE} = 8 MHz and f_{CPU} = 550 MHz

Symbol	Parameter	Conditions	Monitored frequency band	Max	Unit
S_{EMI}	Peak level(1)	V_{DD} = 3.6 V, T_A = 25 °C, LQFP176 package, compliant with IEC61967-2	0.1 to 30 MHz	14	dBµV
			30 to 130 MHz	20	
			130 MHz to 1 GHz	27	
			1 GHz to 2 GHz	17	
	Level(2)		0.1 MHz to 2 GHz	2.5	-

1. Refer to AN1709 "EMI radiated test" chapter.
2. Refer to AN1709 "EMI level classification" chapter.

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 48. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C conforming to ANSI/ESDA/JEDEC JS-001	All packages	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-002	All LQFP packages	C1	250	
			All BGA and WLCSP packages	C2a	500	

1. Guaranteed by characterization results.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with JESD78 IC latchup standard.

Table 49. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latchup class	Conforming to JESD78, $T_J = T_{JMax}$	II level A

6.3.15 I/O current injection characteristics

As a general rule, a current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during the normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

The following tables are the compilation of the SIC1/SIC2 and functional ESD results.

Negative induced A negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

Table 50. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	PA12, PE8	5	0	mA
	PC4, PE12, PF15, PH0	0	NA	
	PA0, PA0_C, PA1, PA1_C, PC2, PC2_C, PC3, PC3_C, PA4, PA5, PE7, PG1, PH4, PH5, BOOT0	0	0	
	All other I/Os	5	NA	

1. Guaranteed by characterization results.

6.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 51: I/O static characteristics* are derived from tests performed under the conditions summarized in *Table 12: General operating conditions*. All I/Os are CMOS and TTL compliant (except for BOOT0).

Note: For information on GPIO configuration, refer to application note AN4899 "STM32 GPIO configuration for hardware settings and low-power consumption", available from the ST website www.st.com.

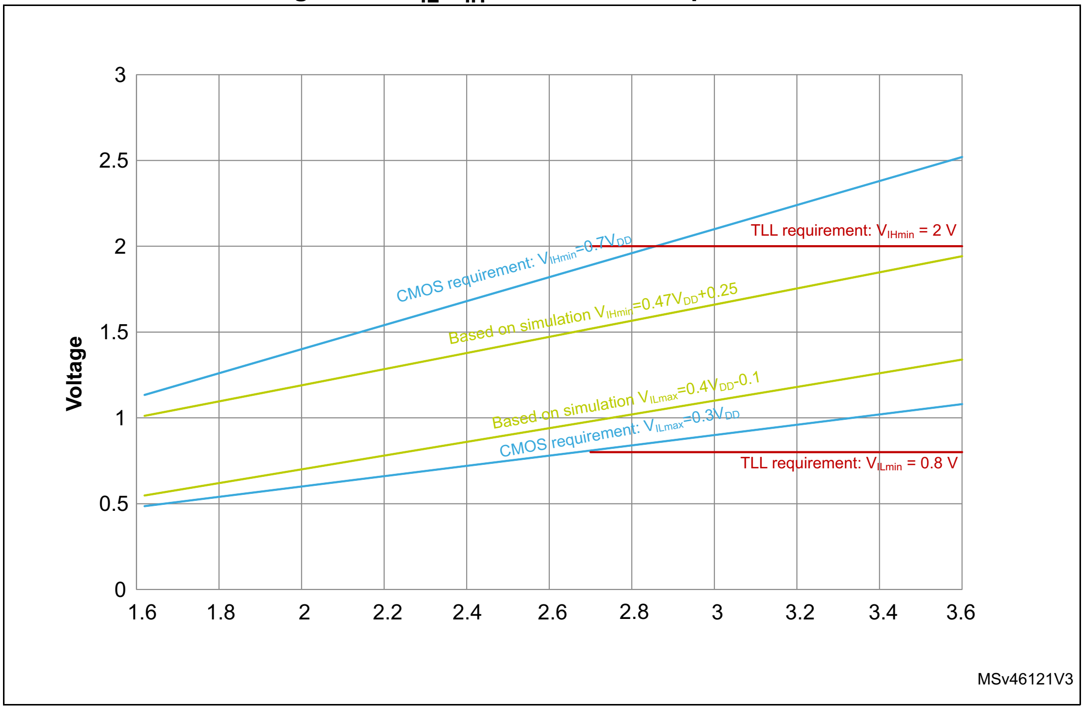
Table 51. I/O static characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage except BOOT0	1.62 V<V_{DD}<3.6 V	-	-	$0.3V_{DD}$(1)	V
	I/O input low level voltage except BOOT0		-	-	$0.4V_{DD}-0.1$(2)	
	BOOT0 I/O input low level voltage		-	-	$0.19V_{DD}+0.1$(2)	
V_{IH}	I/O input high level voltage except BOOT0 and Pxy_C I/Os	1.62 V<V_{DD}<3.6 V	$0.7V_{DD}$(1)	-	-	V
	Pxy_C pin input high level voltage		$0.7V_{DD}$(3)			
	I/O input high level voltage except BOOT0		$0.47V_{DD}+0.25$(2)	-	-	
	BOOT0 I/O input high level voltage		$0.17V_{DD}+0.6$(2)	-	-	
V_{HYS}(2)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V< V_{DD} <3.6 V	-	250	-	mV
	BOOT0 I/O input hysteresis		-	200	-	
I_{lkg}(4)	FT_xx Input leakage current(2)	0< V_{IN} ≤ Max(V_{DDXXX})(9)	-	-	+/-250	nA
		Max(V_{DDXXX}) < V_{IN} ≤ 5.5 V (5)(6)(9)	-	-	1500	
	FT_u IO	0< V_{IN} ≤ Max(V_{DDXXX})(9)	-	-	+/- 350	
		Max(V_{DDXXX}) < V_{IN} ≤ 5.5 V (5)(6)(9)	-	-	5000(7)	
	TT_xx Input leakage current	0< V_{IN} ≤ Max(V_{DDXXX}) (9)	-	-	+/-250	
	VPP (BOOT0 alternate function)	0< V_{IN} ≤ V_{DD}	-	-	15	
		V_{DD} < V_{IN} ≤ 9 V			35	
R_{PU}	Weak pull-up equivalent resistor(8)	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(8)	V_{IN}=V_{DD}(9)	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Compliant with CMOS requirements.
2. Guaranteed by design.
3. To use these I/Os in digital input mode, V_{DD} must respect the following condition: 0.7 V_{DD} < V_{DDA} + 0.3 V.
4. This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula: $I_{Total\_leak\_max}$ = 10 µA + [number of I/Os where V_{IN} is applied on the pad] x $I_{lkg(Max)}$.
5. All FT_xx IO except FT_lu, FT_u and PC3.
6. V_{IN} must be less than Max(VDDXXX) + 3.6 V.
7. To sustain a voltage higher than MIN(V_{DD}, V_{DDA}, $V_{DD33USB}$) +0.3 V, the internal pull-up and pull-down resistors must be disabled.
8. The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).
9. Max(VDDXXX) is the maximum value of all the I/O supplies.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 17*.

Figure 17. V_{IL}/V_{IH} for all I/Os except BOOT0



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 10*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 10*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 52: Output voltage characteristics for all I/Os except PC13, PC14 and PC15* and *Table 53: Output voltage characteristics for PC13, PC14 and PC15* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 12: General operating conditions*. All I/Os are CMOS and TTL compliant.

Table 52. Output voltage characteristics for all I/Os except PC13, PC14 and PC15(1)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO} = 8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO} = −8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} − 0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO} = 8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	TTL port(2) I_{IO} = −8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.3	
V_{OH}(3)	Output high level voltage	I_{IO} = −20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} − 1.3	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 4 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage	I_{IO} = −4 mA 1.62 V ≤V_{DD} < 3.6 V	V_{DD} − 0.4	-	
V_{OL}(3)	Output low level voltage for Pxy_C pins	I_{IO} = 1 mA 1.62 V ≤ V_{DD} < 3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage for Pxy_C pins(4)	I_{IO} = 1 mA 1.62 V ≤ V_{DD} < 3.6 V	Min(V_{DD} − 0.4, V_{DDA} + 0.3)	-	
V_{OLFM+}(3)	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO} = 20 mA 2.3 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
		I_{IO} = 10 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	-	0.4	

1. The IIO current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 9: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.
4. If V_{DDA} + 0.3V < V_{DD} - 0.4 V, an injection current from V_{DD} to V_{DDA} can be observed that can perturb the analog peripherals.

Table 53. Output voltage characteristics for PC13, PC14 and PC15[(1)]

Symbol	Parameter	Conditions[(3)]	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port[(2)] I_{IO} = 3 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port[(2)] I_{IO} = −3 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD}−0.4	-	
V_{OL}[(3)]	Output low level voltage	TTL port[(2)] I_{IO} = 3 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}[(2)]	Output high level voltage	TTL port[(2)] I_{IO} = −3 mA 2.7 V≤ V_{DD} ≤3.6 V	2.4	-	
V_{OL}[(2)]	Output low level voltage	I_{IO} = 1.5 mA 1.62 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}[(2)]	Output high level voltage	I_{IO} = −1.5 mA 1.62 V≤ V_{DD} ≤3.6 V	V_{DD}−0.4	-	

1. The IIO current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 9: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Output buffer timing characteristics (HSLV option disabled)

The HSLV bit of SYSCFG_CCCSR register can be used to optimize the I/O speed when the product voltage is below 2.7 V.

Table 54. Output timing characteristics (HSLV OFF)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	12	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	12	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	16	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	4	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	16.6	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	33.3	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	13.3	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	25	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	20	
01	F_{max}(2)	Maximum frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	60	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	15	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	80	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	15	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	110	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	20	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	5.2	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	4.2	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	7.5	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	2.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	5.2	

Table 54. Output timing characteristics (HSLV OFF)(1) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
10	F_{max}(2)	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	85	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	35	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	110	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	40	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	166	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	100	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	3.8	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	6.9	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	2.8	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	5.2	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	1.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(v)	-	3.3	
11	F_{max}(2)	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(v)	-	100	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	50	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(v)	-	133	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	66	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	220	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	85	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	3.3	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	6.6	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	2.4	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	4.5	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	1.5	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	2.7	

1. Guaranteed by design.
2. The maximum frequency is achieved with a duty cycle of 45 to 55 %, when loaded by the specified capacitance.
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

Output buffer timing characteristics (HSLV option enabled)

Table 55. Output timing characteristics (HSLV ON)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	11	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	9	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	6.6	
01	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	50	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	58	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	66	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	6.6	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	4.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
10	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	55	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	80	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	133	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	5.8	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	4	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	2.4	
11	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	60	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	90	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	175	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	5.3	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	3.6	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	1.9	

1. Guaranteed by design.
2. The maximum frequency is achieved with a duty cycle of 45 to 55 %, when loaded by the specified capacitance.
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

Analog switch between ports Pxy_C and Pxy

PA0_C, PA1_C, PC2_C and PC3_C can be connected internally to PA0, PA1, PC2 and PC3, respectively (refer to SYSCFG_PMCR register in RM0468 reference manual). The switch is controlled by $V_{DDSWITCH}$ voltage level. It is defined through BOOSTVDDSEL bit of SYSCFG_PMCR. If the switch is closed the switch characteristics are given in the table below.

Table 56. Pxy_C and Pxy analog switch characteristics

Parameter	Conditions		Min	Typ	Max	Unit
Switch impedance	Switch control boosted		-	-	315	Ω
	Switch control not boosted	$V_{DDSWITCH}$ > 2.7 V	-	-	315	
		$V_{DDSWITCH}$ > 2.4 V	-	-	335	
		$V_{DDSWITCH}$ > 2.0 V	-	-	390	
		$V_{DDSWITCH}$ > 1.8 V	-	-	445	
		$V_{DDSWITCH}$ > 1.62 V	-	-	550	

6.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 51: I/O static characteristics*).

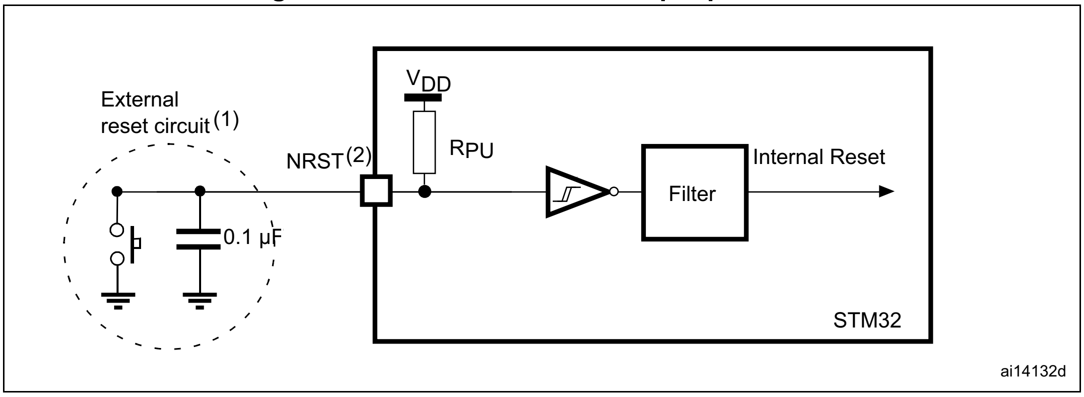
Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 12: General operating conditions*.

Table 57. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}(2)	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse	1.71 V < V_{DD} < 3.6 V	-	-	50	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	1.71 V < V_{DD} < 3.6 V	350	-	-	
		1.62 V < V_{DD} < 3.6 V	1000	-	-	

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Figure 18. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 51*. Otherwise the reset is not taken into account by the device.

6.3.18 FMC characteristics

Unless otherwise specified, the parameters given in *Table 58* to *Table 71* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 12: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5V_{DD}
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS0.

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics.

Asynchronous waveforms and timings

Figure 19 through *Figure 21* represent asynchronous waveforms and *Table 58* through *Table 65* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capacitive load C_L = 30 pF

In all timing tables, the T_{KERCK} is the $f_{mc\_ker\_ck}$ clock period.

Table 58. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings[(1)]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc\_ker\_ck}-1$	$3T_{fmc\_ker\_ck}+1$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{fmc\_ker\_ck}-1$	$2T_{fmc\_ker\_ck}+1$	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc\_ker\_ck}$	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	$2T_{fmc\_ker\_ck}$	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{fmc\_ker\_ck}+14$	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	13	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	4	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc\_ker\_ck}+1$	

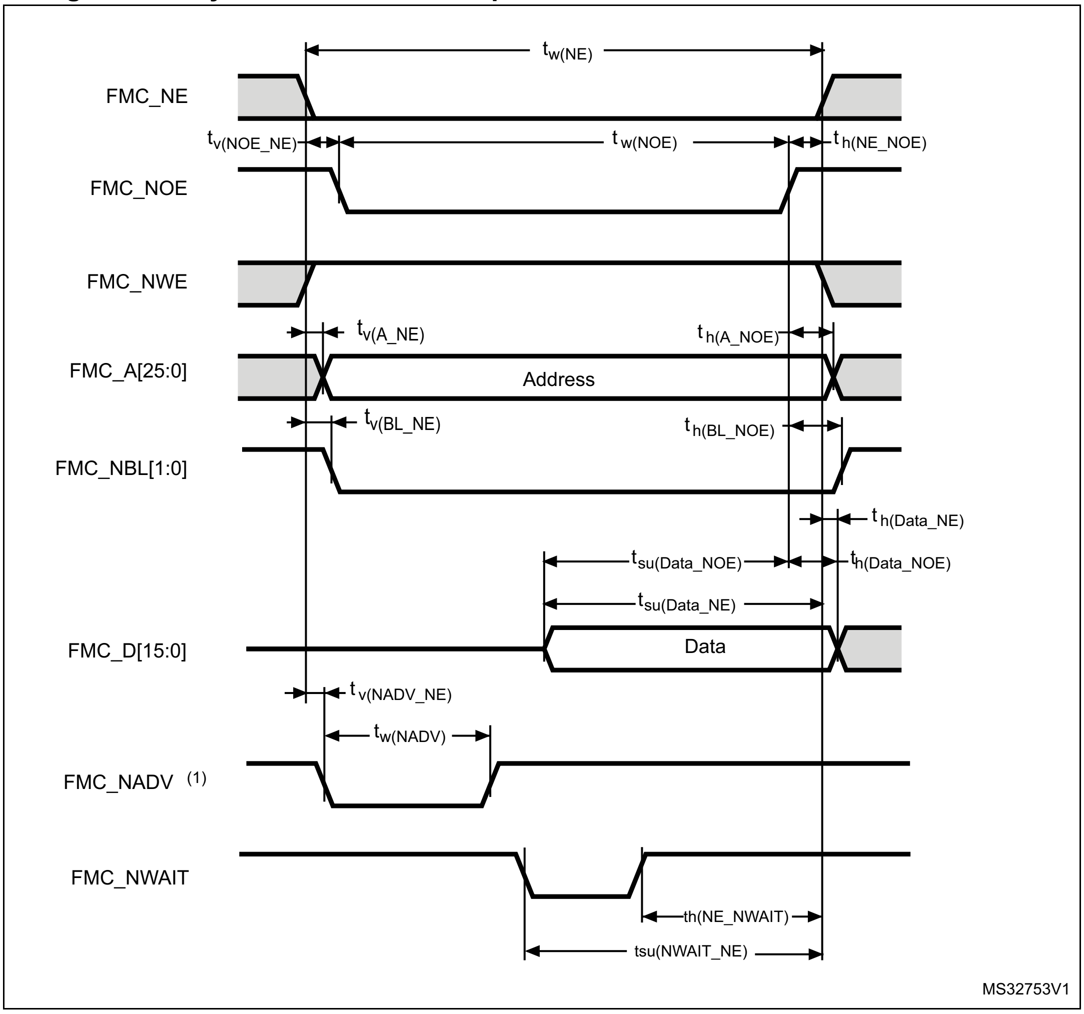
1. Guaranteed by characterization results.

Table 59. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings[(1)(2)]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{fmc\_ker\_ck}-1$	$7T_{fmc\_ker\_ck}+1$	ns
$t_{w(NOE)}$	FMC_NOE low time	$5T_{fmc\_ker\_ck}-1$	$5T_{fmc\_ker\_ck}+1$	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{fmc\_ker\_ck}-0.5$	-	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$4T_{fmc\_ker\_ck}+9$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$3T_{fmc\_ker\_ck}+12$	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 fmc_ker_ck cycle.

Figure 19. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 60. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc\_ker\_ck} - 1$	$3T_{fmc\_ker\_ck} + 1$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc\_ker\_ck} - 1$	$T_{fmc\_ker\_ck}$	
$t_{w(NWE)}$	FMC_NWE low time	$T_{fmc\_ker\_ck} - 0.5$	$T_{fmc\_ker\_ck} + 0.5$	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc\_ker\_ck}$	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	1	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{fmc\_ker\_ck} + 2$	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc\_ker\_ck}$	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	5	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc\_ker\_ck} + 1$	

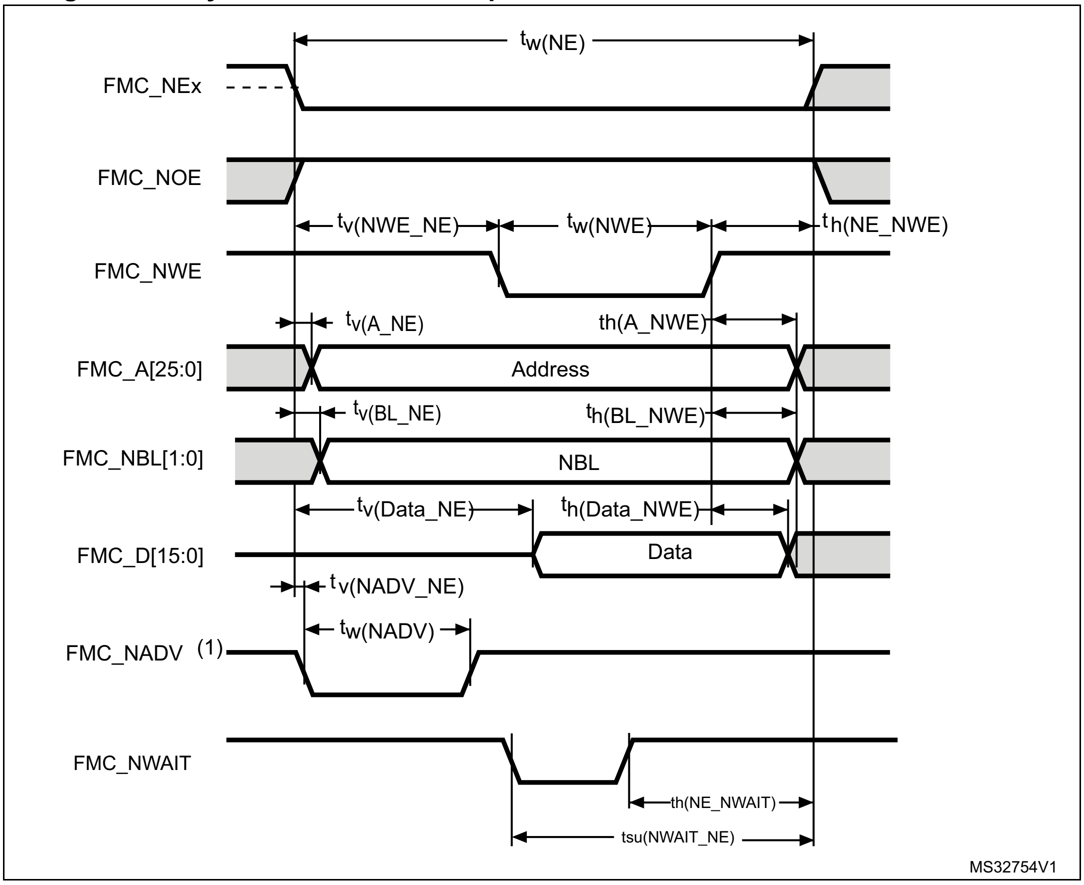
1. Guaranteed by characterization results.

Table 61. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc\_ker\_ck} - 1$	$8T_{fmc\_ker\_ck} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{fmc\_ker\_ck} - 1$	$6T_{fmc\_ker\_ck} + 1$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc\_ker\_ck} + 13$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc\_ker\_ck} + 12$	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 fmc_ker_ck cycle.

Figure 20. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 62. Asynchronous multiplexed PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc\_ker\_ck} - 1$	$4T_{fmc\_ker\_ck} + 1$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{fmc\_ker\_ck}$	$2T_{fmc\_ker\_ck} + 0.5$	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{fmc\_ker\_ck} - 1$	$T_{fmc\_ker\_ck} + 1$	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc\_ker\_ck}$	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	4.0	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc\_ker\_ck} - 0.5$	$T_{fmc\_ker\_ck} + 1$	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high)	$T_{fmc\_ker\_ckk} - 4$	-	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{fmc\_ker\_ck} + 14$	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	13	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Guaranteed by characterization results.

Table 63. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc\_ker\_ck} - 1$	$8T_{fmc\_ker\_ck} + 1$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{fmc\_ker\_ck} - 1$	$5T_{fmc\_ker\_ck} + 1$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$4T_{fmc\_ker\_ck} + 9$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$3T_{fmc\_ker\_ck} + 12$	-	

1. Guaranteed by characterization results.

Figure 21. Asynchronous multiplexed PSRAM/NOR read waveforms

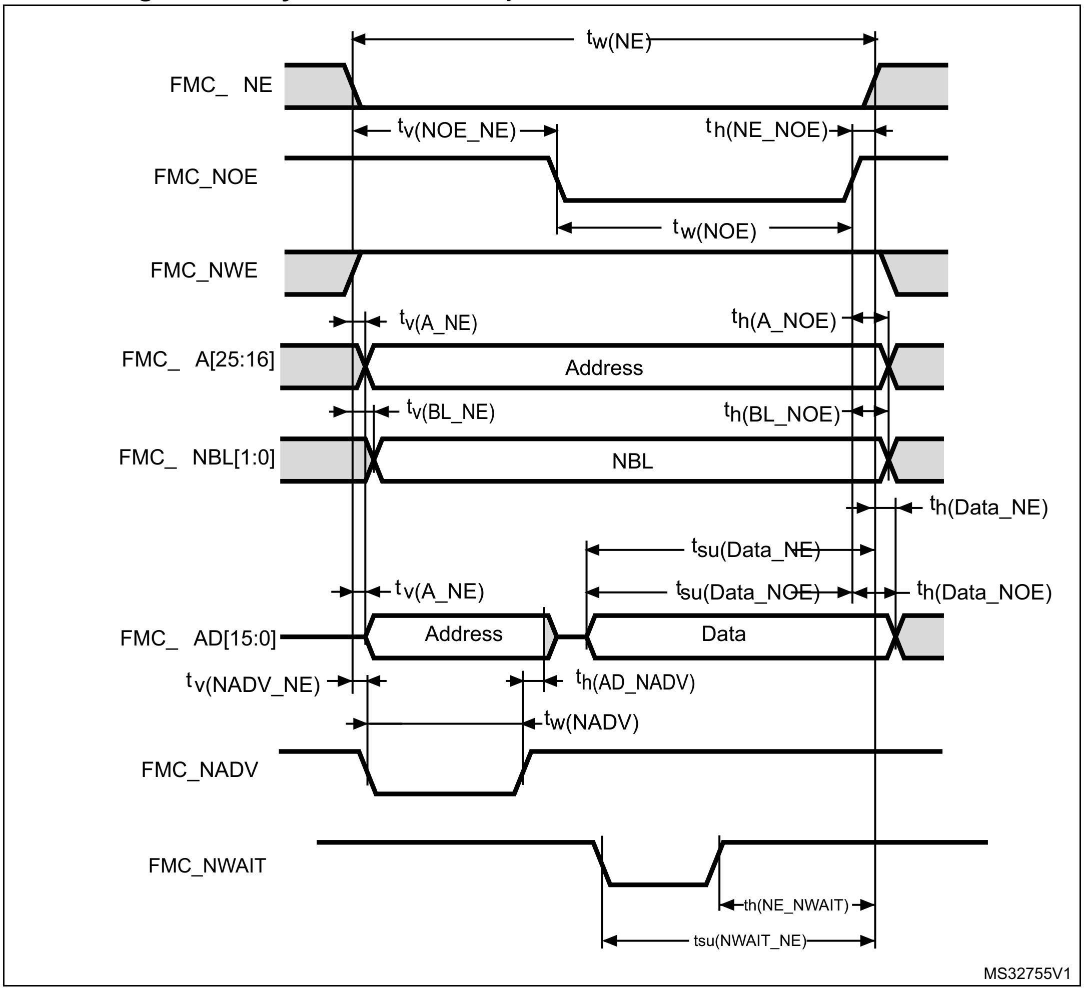


Table 64. Asynchronous multiplexed PSRAM/NOR write timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc\_ker\_ck} - 1$	$4T_{fmc\_ker\_ck}$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc\_ker\_ck} - 1$	$T_{fmc\_ker\_ck} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{fmc\_ker\_ck} - 0.5$	$2T_{fmc\_ker\_ck} + 0.5$	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	1	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	5.0	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc\_ker\_ck} - 0.5$	$T_{fmc\_ker\_ck} + 1$	
$t_{h(AD\_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high)	$T_{fmc\_ker\_ck} - 4.5$	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	$T_{fmc\_ker\_ck} + 2$	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc\_ker\_ck}$	-	

1. Guaranteed by characterization results.

Table 65. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings[1][2]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{fmc\_ker\_ck} - 1$	$9T_{fmc\_ker\_ck}$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{fmc\_ker\_ck} - 0.5$	$7T_{fmc\_ker\_ck} + 0.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc\_ker\_ck} + 9$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc\_ker\_ck} + 12$	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 fmc_ker_ck cycle.

Synchronous waveforms and timings

Figure 24 through *Figure 23* represent synchronous waveforms and *Table 68* through *Table 67* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR flash, DataLatency = 0 for PSRAM, C_L = 30 pF

In all the timing tables, the $T_{fmc\_ker\_ck}$ is the $f_{mc\_ker\_ck}$ clock period, with the following FMC_CLK maximum values:

- For 2.7 V<V_{DD}<3.6 V: maximum FMC_CLK = 137 MHz at C_L = 20 pF
- For 1.8 V<V_{DD}<1.9 V: maximum FMC_CLK = 100 MHz at C_L = 20 pF
- For 1.62 V<V_{DD}<1.8 V: maximumFMC_CLK = 88 MHz at C_L = 15 pF

Table 66. Synchronous non-multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter		Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period		$2T_{fmc\_ker\_ck}$ –0.5	-	ns
$t_{(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)		-	3	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)		$T_{fmc\_ker\_ck}$+1.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	1.62 V <V_{DD} < 3.6 V	-	5.5	
		2.7 V <V_{DD} < 3.6 V		2.0	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1.62 V <V_{DD} < 3.6 V	1	-	
		2.7 V <V_{DD} < 3.6 V		-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)		-	3	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)		$T_{fmc\_ker\_ck}$	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK ow to FMC_NOE low		-	2.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high		$T_{fmc\_ker\_ck}$+1	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high		3	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high		0	-	
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high		3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high		2.5	-	

1. Guaranteed by characterization results.

Figure 22. Synchronous non-multiplexed NOR/PSRAM read timings

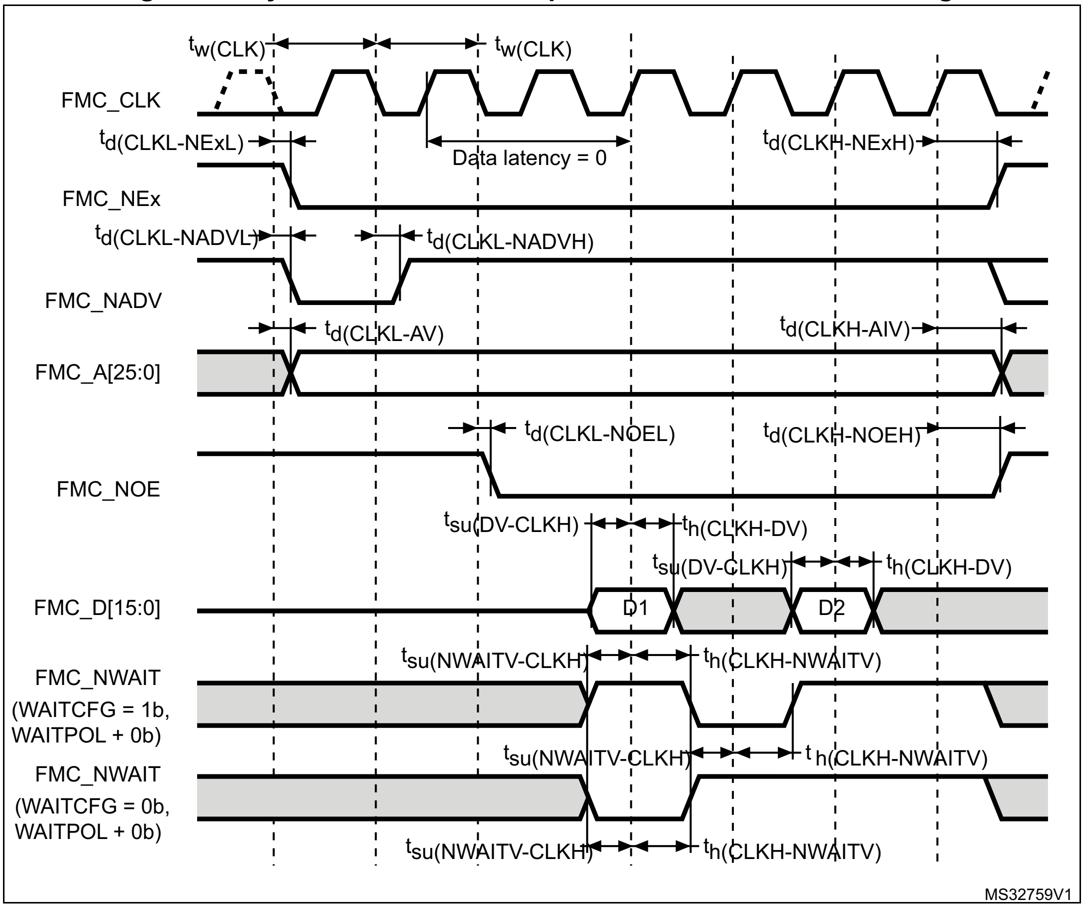


Table 67. Synchronous non-multiplexed PSRAM write timings(1)

Symbol	Parameter		Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period		$2T_{fmc\_ker\_ck} - 0.5$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)		-	3	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)		$T_{fmc\_ker\_ck}+1.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	1.62 V <V_{DD} < 3.6 V	-	5.5	
		2.7 V <V_{DD} < 3.6 V		2	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1.62 V <V_{DD} < 3.6 V	1	-	
		2.7 V <V_{DD} < 3.6 V		-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)		-	3	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)		$T_{fmc\_ker\_ck}$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low		-	2.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high		$T_{fmc\_ker\_ck}+1$	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low		-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low		-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high		$T_{fmc\_ker\_ck}+0.5$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high		3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high		2.5	-	

1. Guaranteed by characterization results.

Figure 23. Synchronous non-multiplexed PSRAM write timings

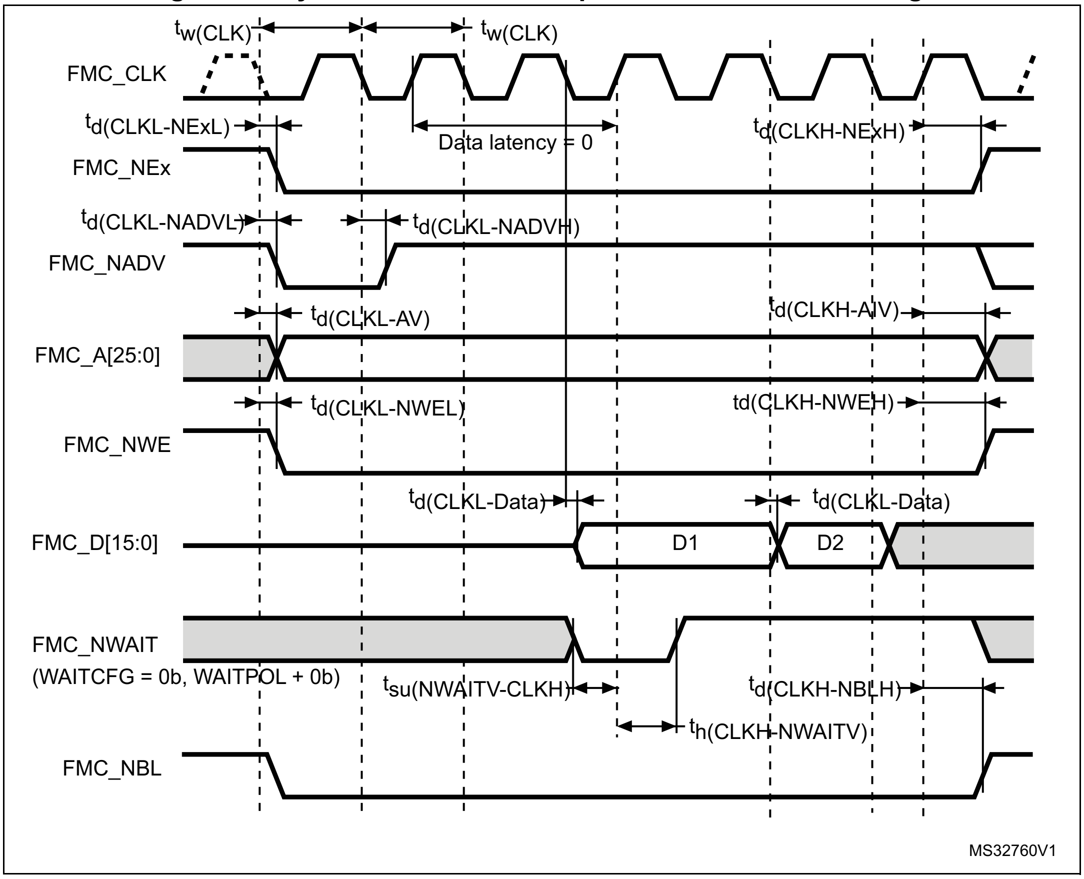


Table 68. Synchronous multiplexed NOR/PSRAM read timings[1]

Symbol	Parameter		Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period		$2T_{fmc\_ker\_ck} - 0.5$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)		-	3	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)		$T_{fmc\_ker\_ck}+1.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	1.62 V <V_{DD} < 3.6 V	-	5.5	
		2.7 V <V_{DD} < 3.6 V		2	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1.62 V <V_{DD} < 3.6 V	1	-	
		2.7 V <V_{DD} < 3.6 V		-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)		-	3	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)		$T_{fmc\_ker\_ck}$	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low		-	2.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high		$T_{fmc\_ker\_ck}+1$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid		-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid		0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high		3	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high		0	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high		3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high		2.5	-	

1. Guaranteed by characterization results.

Figure 24. Synchronous multiplexed NOR/PSRAM read timings

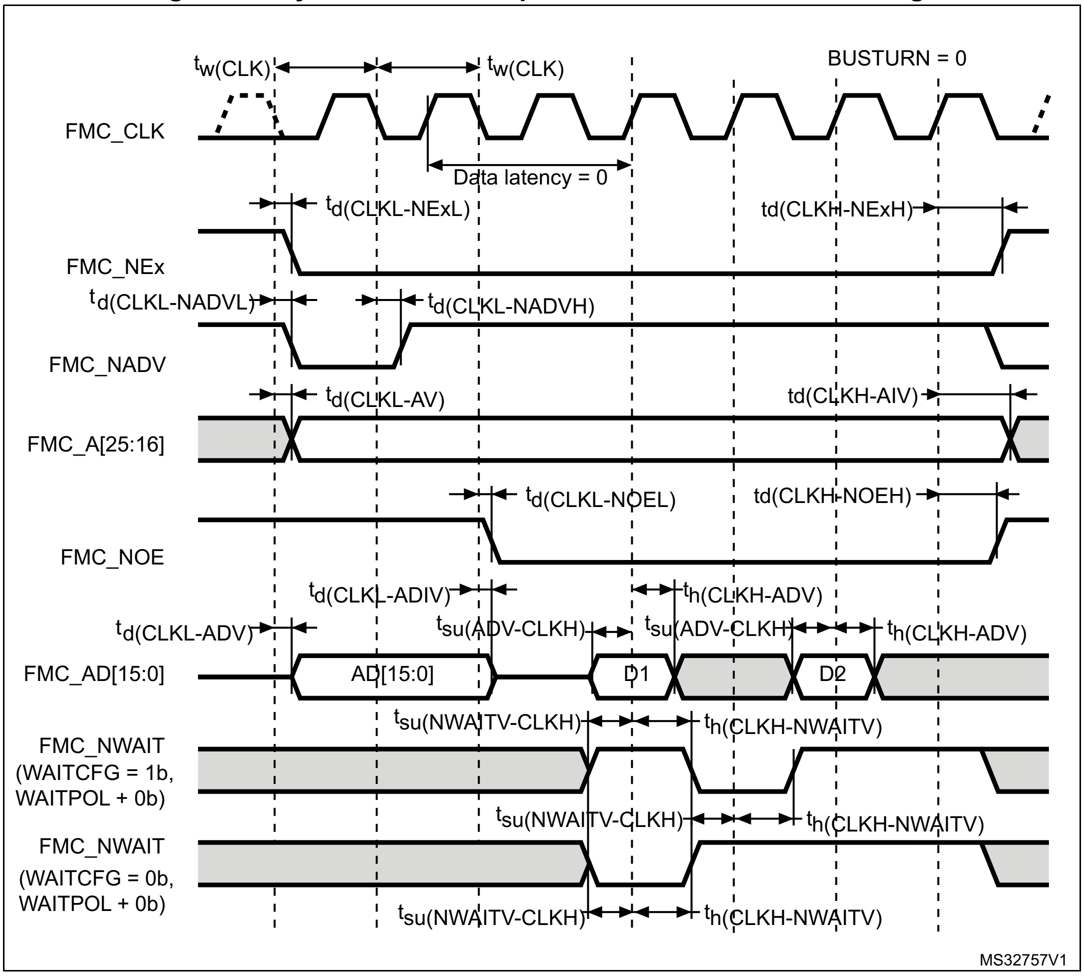
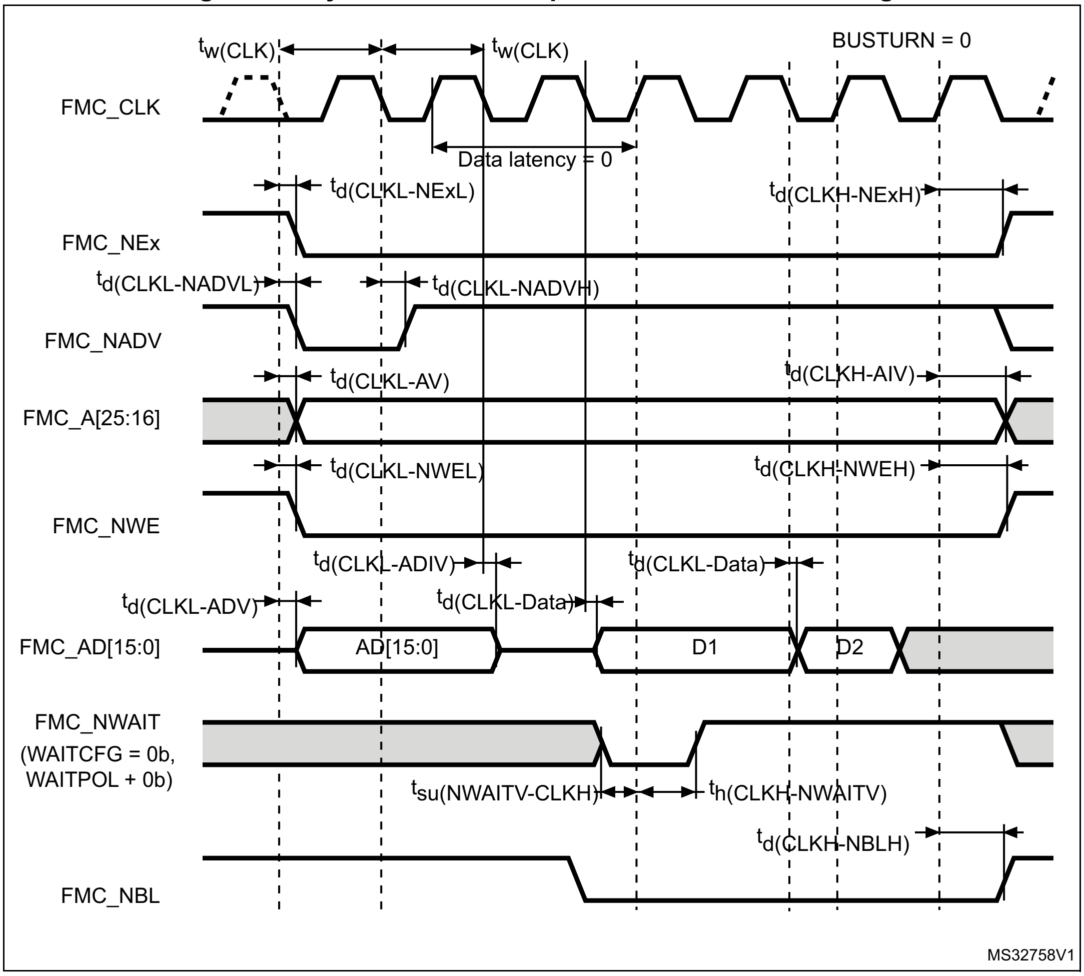


Table 69. Synchronous multiplexed PSRAM write timings(1)

Symbol	Parameter		Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period, V_{DD} = 2.7 to 3.6 V		$2T_{fmc\_ker\_ck}$ –0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x =0..2)		-	3	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0…2)		$T_{fmc\_ker\_ck}$ +1.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	1.62 V <V_{DD} < 3.6 V	-	5.5	
		2.7 V <V_{DD} < 3.6 V		2.0	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1.62 V <V_{DD} < 3.6 V	1	-	
		2.7 V <V_{DD} < 3.6 V		-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x =16…25)		-	3	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x =16…25)		$T_{fmc\_ker\_ck}$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low		-	2.5	
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high		$T_{fmc\_ker\_ck}$ +1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to to FMC_AD[15:0] valid		-	2.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid		0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low		-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low		-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high		$T_{fmc\_ker\_ck}$ +0.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high		3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high		2.5	-	

1. Guaranteed by characterization results.

Figure 25. Synchronous multiplexed PSRAM write timings



NAND controller waveforms and timings

Figure 26 through Figure 29 represent synchronous waveforms, and Table 70 and Table 71 provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration and a capacitive load (C_L) of 30 pF:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0

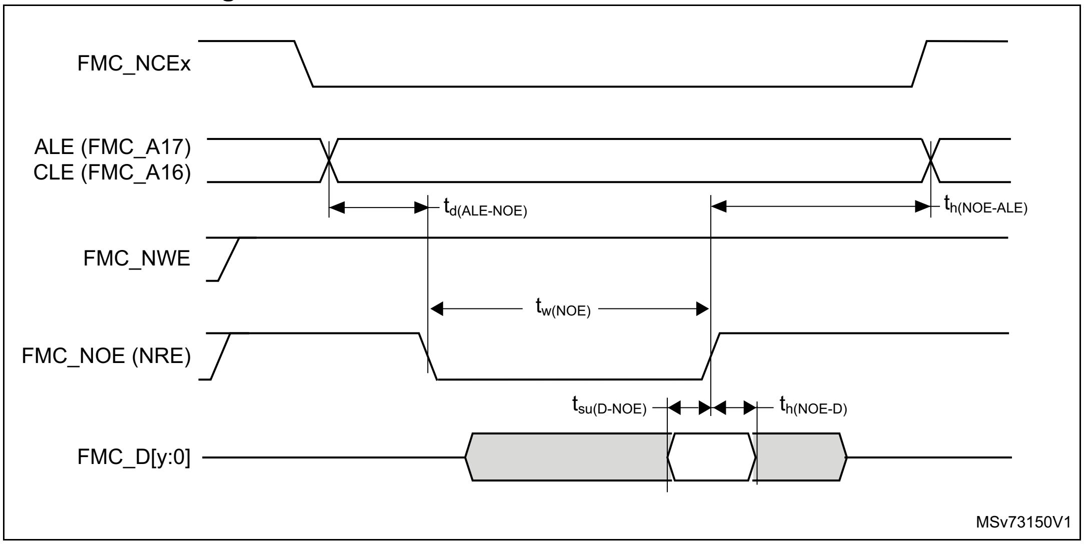
In all timing tables, the $T_{fmc\_ker\_ck}$ is the fmc_ker_ck clock period.

Table 70. Switching characteristics for NAND flash read cycles[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(NOE)}$	FMC_NOE low width	$4T_{fmc\_ker\_ck} - 0.5$	$4T_{fmc\_ker\_ck} + 0.5$	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	11	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$3T_{fmc\_ker\_ck} + 0.5$	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$4T_{fmc\_ker\_ck} - 1$	-	

1. Guaranteed by characterization results.

Figure 26. NAND controller waveforms for read access



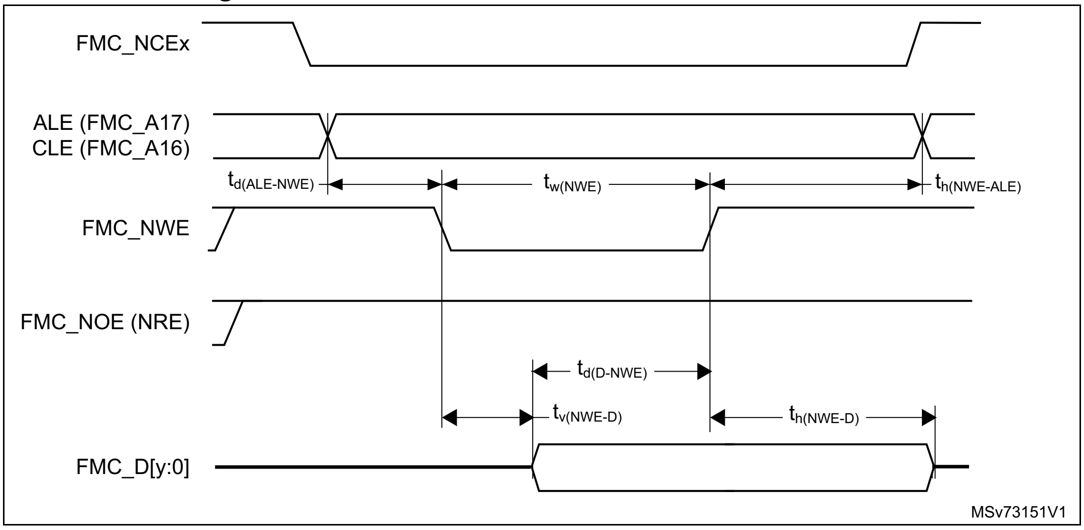
1. y = 7 or 15 depending on the NAND flash memory interface.

Table 71. Switching characteristics for NAND flash write cycles[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{fmc\_ker\_ck} - 0.5$	$4T_{fmc\_ker\_ck} + 0.5$	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{fmc\_ker\_ck} + 1.5$	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{fmc\_ker\_ck} - 5$	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	$3T_{fmc\_ker\_ck} + 0.5$	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{fmc\_ker\_ck} - 0.5$	-	

1. Guaranteed by characterization results.

Figure 27. NAND controller waveforms for write access



1. y = 7 or 15 depending on the NAND flash memory interface.

SDRAM waveforms and timings

In all timing tables, the TKERCK is the fmc_ker_ck clock period, with the following FMC_SDCLK maximum values:

- For 2.7 V<V_{DD}<3.6 V: maximum FMC_CLK = 95 MHz at 20 pF
- For 1.8 V<V_{DD}<1.9 V: maximum FMC_CLK = 90 MHz at 20 pF
- For 1.62 V<$_{DD}$<1.8 V: maximum FMC_CLK = 85 MHz at 15 pF

Table 72. SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck}$ – 0.5	$2T_{fmc\_ker\_ck}$ +0.5	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	3	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	1.5	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	2.0	
$t_{d(SDCLKL-SDNE)}$	Chip select valid time	-	1.5(2)	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	2.0	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0.5	-	

1. Guaranteed by characterization results.
2. Using PC2_C I/O adds 4.5 ns to this timing.

Table 73. LPSDR SDRAM read timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 0.5$	$2T_{fmc\_ker\_ck}+0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	3	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	2.5	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	2	
$t_{d(SDCLKL\_SDNE)}$	Chip select valid time	-	1.5[2][3]	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	2	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0.5	-	

1. Guaranteed by characterization results.
2. Using PC2 I/O adds 4 ns to this timing.
3. Using PC2_C I/O adds 16.5 ns to this timing.

Figure 28. SDRAM read access waveforms (CL = 1)

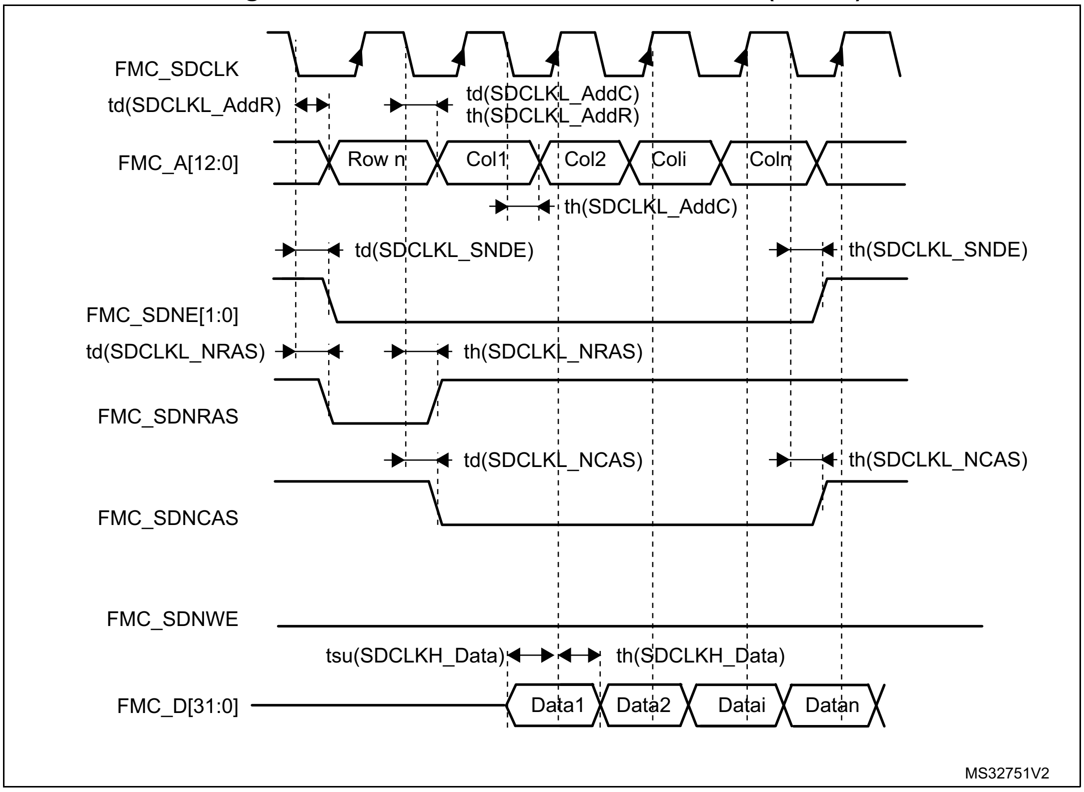


Table 74. SDRAM Write timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 0.5$	$2T_{fmc\_ker\_ck}+0.5$	ns
$t_{d(SDCLKL\_Data)}$	Data output valid time	-	2	
$t_{h(SDCLKL\_Data)}$	Data output hold time	0.5	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	2	
$t_{d(SDCLKL\_SDNWE)}$	SDNWE valid time	-	2	
$t_{h(SDCLKL\_SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL\_SDNE)}$	Chip select valid time	-	1.5[2]	
$t_{h(SDCLKL-\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	2	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0.5	-	

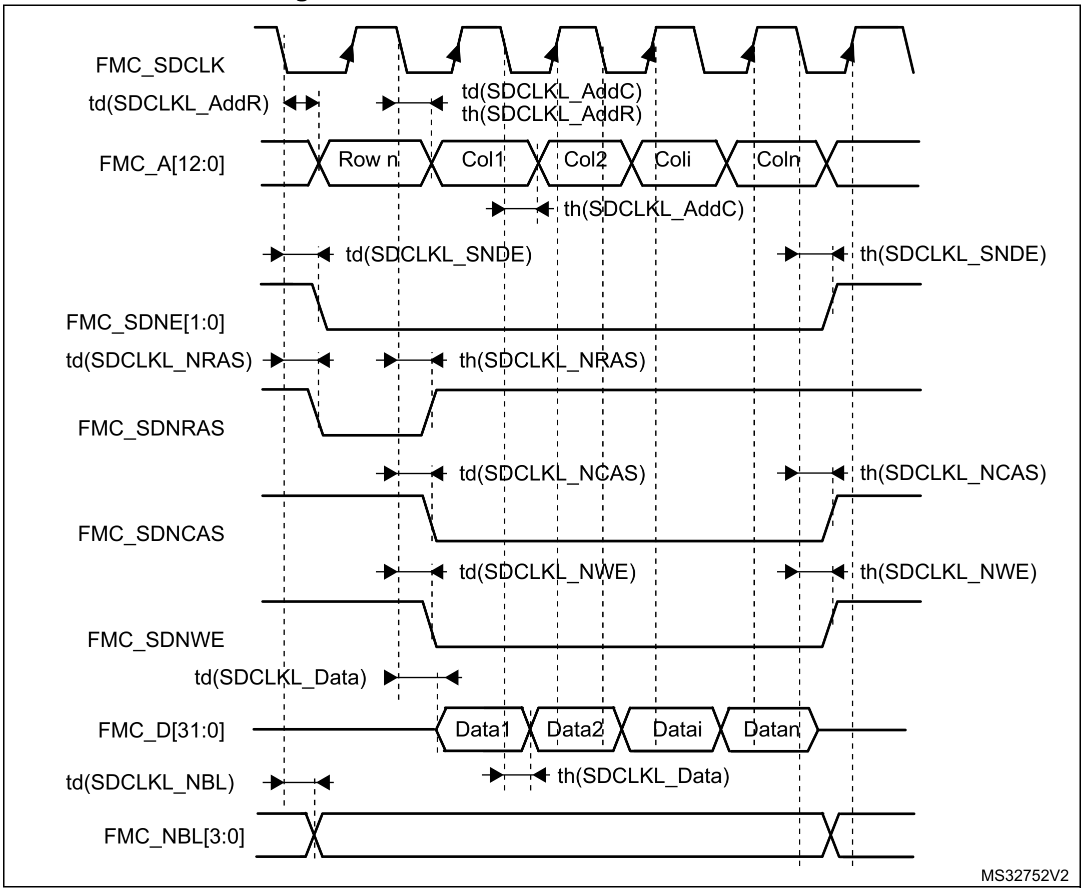
1. Guaranteed by characterization results.
2. Using PC2_C I/O adds 4.5 ns to this timing.

Table 75. LPSDR SDRAM Write timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 0.5$	$2T_{fmc\_ker\_ck}+0.5$	ns
$t_{d(SDCLKL\_Data)}$	Data output valid time	-	2	
$t_{h(SDCLKL\_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	2.5	
$t_{d(SDCLKL-SDNWE)}$	SDNWE valid time	-	2	
$t_{h(SDCLKL-SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL-SDNE)}$	Chip select valid time	-	1.5[2][3]	
$t_{h(SDCLKL-SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	2	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS hold time	0.5	-	

1. Guaranteed by characterization results.
2. Using PC2 I/O adds 4 ns to this timing.
3. Using PC2_C I/O adds 16.5 ns to this timing.

Figure 29. SDRAM write access waveforms



6.3.19 Octo-SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 76* and *Table 78* for OCTOSPI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 12: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.5$ V
- VOS level set to VOS0

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 76. OCTOSPI characteristics in SDR mode(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{(CLK)}$	OCTOSPI clock frequency	1.71 V < V_{DD} < 3.6 V, VOS0, C_{LOAD} = 15 pF	-	-	92	MHz
		1.71 V < V_{DD} < 3.6 V, VOS0, C_{LOAD} =20 pF	-	-	90	
		2.7 V < V_{DD} < 3.6 V, VOS0, C_{LOAD} = 20 pF	-	-	140	
$t_{w(CKH)}$	OCTOSPI clock high and low time, even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	ns
$t_{w(CKL)}$			$t_{(CK)}/2–1$	-	$t_{(CK)}/2$	
$t_{w(CKH)}$	OCTOSPI clock high and low time, odd division	PRESCALER[7:0] = n = 2,4,6,8	$(n/2)*t_{(CK)}/(n+1)$	-	$(n/2)*t_{(CK)}/(n+1)+1$	
$t_{w(CKL)}$			$(n/2+1)*t_{(CK)}/(n+1)–1$	-	$(n/2+1)*t_{(CK)}/(n+1)$	
$t_{s(IN)}$(3)	Data input setup time	-	3.0	-	-	
$t_{h(IN)}$(3)	Data input hold time	-	1.5	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	0.5	1(4)	
$t_{h(OUT)}$	Data output hold time	-	0	-	-	

1. All values apply to Octal and Quad-SPI mode.
2. Guaranteed by characterization results.
3. Delay block bypassed.
4. Using PC2 or PC3 I/O in the data bus adds 4 ns to this timing value.

Figure 30. OCTOSPI SDR read/write timing diagram

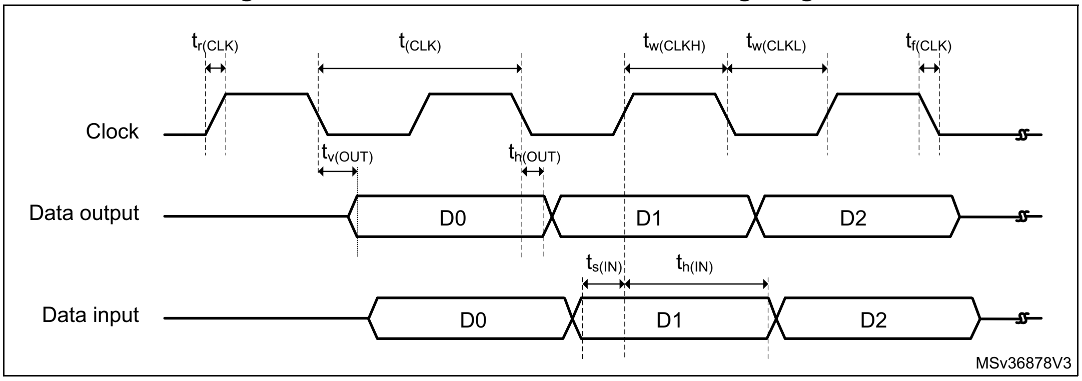


Table 77. OCTOSPI characteristics in DTR mode (no DQS)[1][2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK}[3]	OCTOSPI clock frequency	1.71 V < V_{DD} < 3.6 V, VOS0, C_{LOAD} = 15 pF	-	-	90[4]	MHz
		1.71 V < V_{DD} < 3.6 V, VOS0, C_{LOAD} = 20 pF	-	-	87[4]	
		2.7 V < V_{DD} < 3.6 V, VOS0, C_{LOAD} = 20 pF	-	-	110	
$t_{w(CKH)}$	OCTOSPI clock high and low time, even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	ns
$t_{w(CKL)}$			$t_{(CK)}/2-1$	-	$t_{(CK)}/2$	
$t_{w(CKH)}$	OCTOSPI clock high and low time, odd division	PRESCALER[7:0] = n = 2,4,6,8	$(n/2)*t_{(CK)}/(n+1)$	-	$(n/2)*t_{(CK)}/(n+1)+1$	
$t_{w(CKL)}$			$(n/2+1)*t_{(CK)}/(n+1) - 1$	-	$(n/2+1)*t_{(CK)}/(n+1)$	
$t_{sr(IN)}$, $t_{sf(IN)}$[5]	Data input setup time	-	3.0	-	-	
$t_{hr(IN)}$, $t_{hf(IN)}$[5]	Data input hold time	-	1.50	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time	DHQC = 0	-	6	7[6]	
		DHQC = 1, Prescaler = 1,2 ...	-	$t_{pclk}/4+1$	$t_{pclk}/4+1.25$[6]	
thr(OUT) thf(OUT)	Data output hold time	DHQC = 0	4.5	-	-	
		DHQC = 1, Prescaler = 1,2 ...	$t_{pclk}/4$	-	-	

1. All values apply to Octal and Quad-SPI mode.
2. Guaranteed by characterization results.
3. DHQC must be set to reach the mentioned frequency.
4. Using PC2 or PC3 I/O in the data bus decreases the frequency to 47 MHz.
5. Delay block bypassed.
6. Using PC2 or PC3 I/O in the data bus adds 4 ns to this timing value.

Figure 31. OCTOSPI DTR mode timing diagram

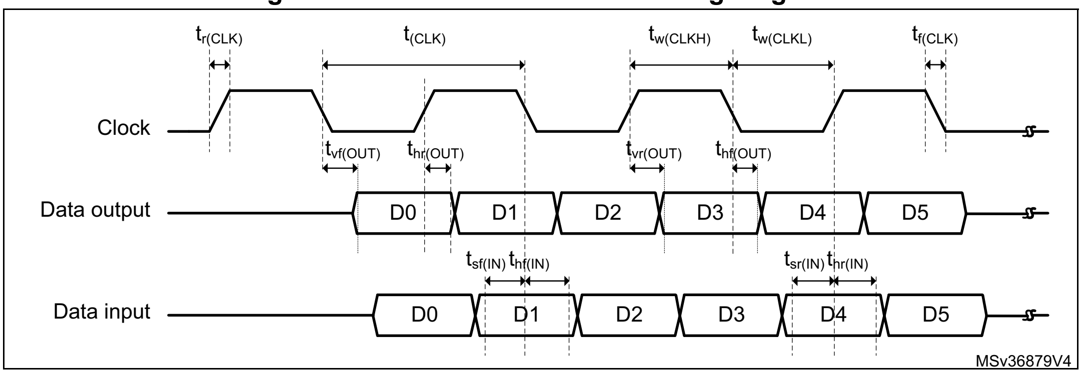


Table 78. OCTOSPI characteristics in DTR mode (with DQS)/Octal and Hyperbus(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK}(2)(3)	OCTOSPI clock frequency	2,7 V < V_{DD} < 3.6 V, VOS0, C_{LOAD} = 20 pF	-	-	100	MHz
		1.71 V < V_{DD} < 3.6 V, VOS0, C_{LOAD} = 20 pF	-	-	100(4)	
$t_{w(CKH)}$	OCTOSPI clock high and low time, even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	ns
$t_{w(CKL)}$			$t_{(CK)}/2-1$	-	$t_{(CK)}/2$	
$t_{w(CKH)}$	OCTOSPI clock high and low time, odd division	PRESCALER[7:0] = n = 2,4,6,8	$(n/2)*t_{(CK)}/(n+1)$	-	$(n/2)*t_{(CK)}/(n+1)+1$	ns
$t_{w(CKL)}$			$(n/2+1)*t_{(CK)}/(n+1)-1$	-	$(n/2+1)*t_{(CK)}/(n+1)$	
$t_{v(CK)}$	Clock valid time	-	-	-	$t_{(CK)}+1$	
$t_{h(CK)}$	Clock hold time	-	$t_{(CK)}/2$	-	-	
$V_{ODr(CK)}$	CK,$\overline{CK}$ crossing level on CK rising edge	VDD = 1.8 V	922	-	1229	mV
$V_{ODf(CK)}$	CK,$\overline{CK}$ crossing level on CK falling edge	VDD = 1.8 V	1000	-	1277	
$t_{w(CS)}$	Chip select high time	-	$3*t_{(CK)}$	-	-	ns
$t_{v(DQ)}$	Data input vallid time	-	0	-	-	
$t_{v(DS)}$	Data strobe input valid time	-	0	-	-	
$t_{h(DS)}$	Data strobe input hold time	-	0	-	-	
$t_{v(RWDS)}$	Data strobe output valid time	-	-	-	3 x $t_{(CK)}$	
$t_{sr(DQ)}$	Data input setup time	Rising edge	0	-	-	
$t_{sf(DQ)}$		Falling edge	0	-	-	
$t_{hr(DQ)}$	Data input hold time	Rising edge	1	-	-	
$t_{hf(DQ)}$		Falling edge	1	-	-	
$t_{vr(OUT)}$	Data output valid time rising edge	DHQC = 0	-	6	7(5)	
		DHQC = 1, Prescaler = 1,2...	-	$t_{pclk}/4+1$	$t_{pclk}/4+1.25$(5)	
$t_{vf(OUT)}$	Data output valid time falling edge	DHQC = 0	-	5.5	6(5)	
		DHQC = 1, Prescaler = 1,2...	-	$t_{pclk}/4+0.5$	$t_{pclk}/4+0.75$(5)	
$t_{hr(OUT)}$	Data output hold time rising edge	DHQC = 0	4.5	-	-	
		DHQC = 1, Prescaler = 1,2...	$t_{pclk}/4$	-	-	
$t_{hf(OUT)}$	Data output hold time falling edge	DHQC = 0	4.5	-	-	
		DHQC = 1, Prescaler = 1,2...	$t_{pclk}/4$	-	-	

1. Guaranteed by characterization results.

2. Maximum frequency values are given for a RWDS to DQ skew of maximum +/-1.0 ns.
3. Activating DHQC is mandatory to reach this frequency
4. Using PC2 or PC3 I/O on data bus decreases the frequency to 47 MHz.
5. Using PC2 or PC3 I/O on the data bus adds 4 ns to this timing value.

Figure 32. OCTOSPI Hyperbus clock timing diagram

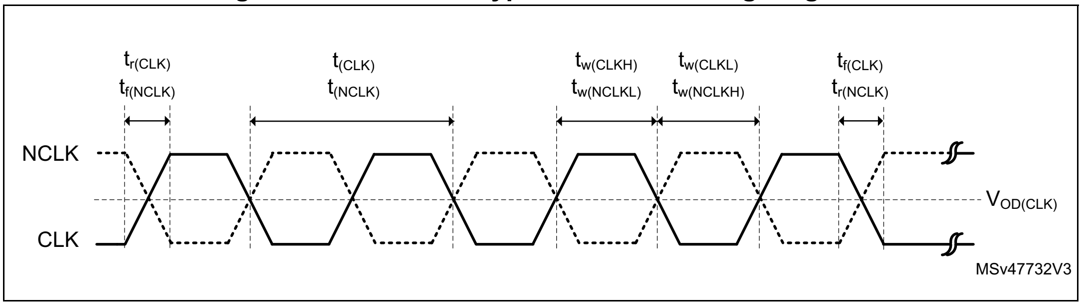


Figure 33. OCTOSPI Hyperbus read timing diagram

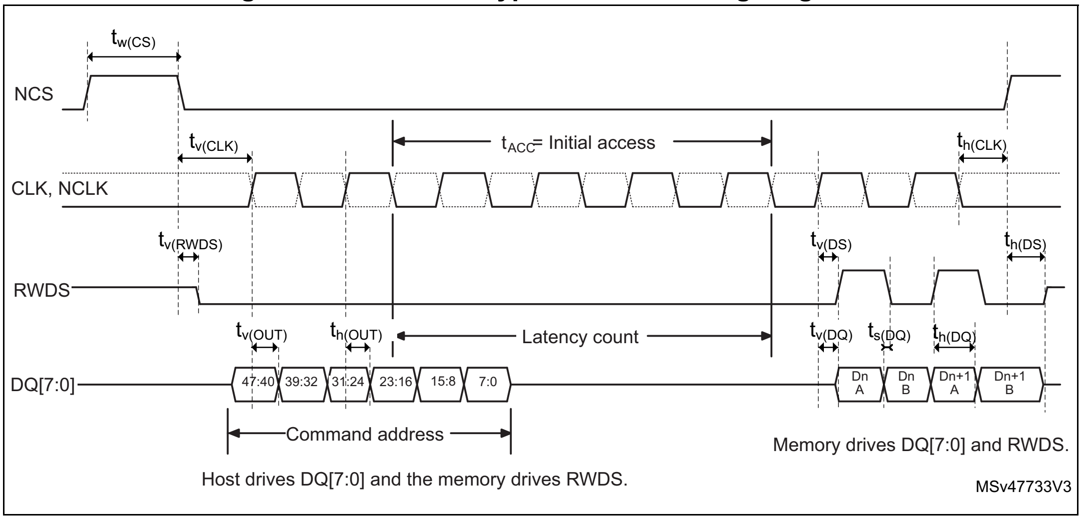
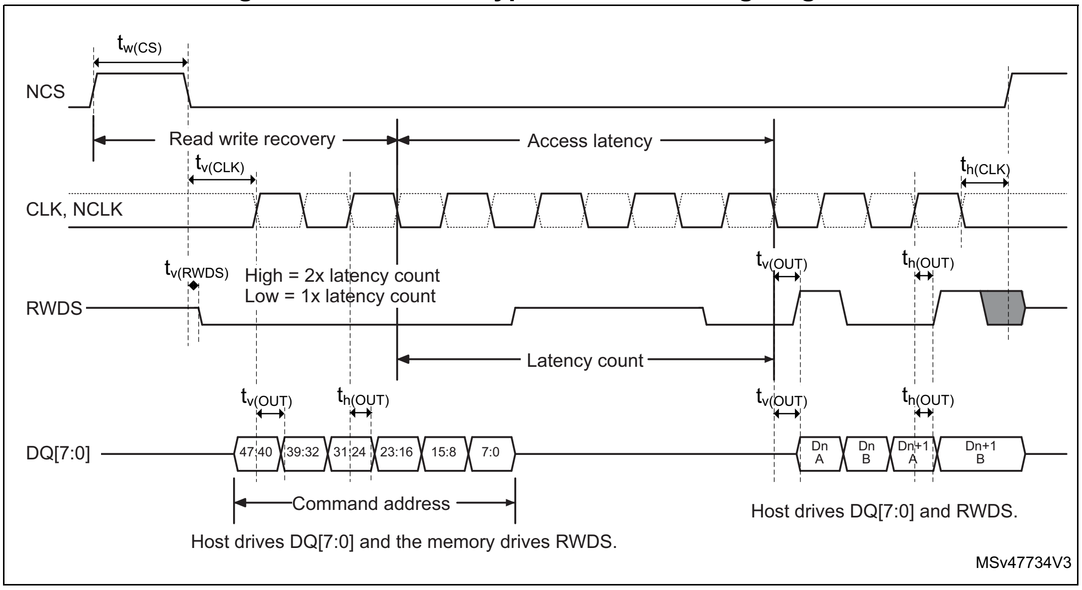


Figure 34. OCTOSPI Hyperbus write timing diagram



6.3.20 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in *Table 79* for Delay Block are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and VDD supply voltage summarized in *Table 12: General operating conditions*, with the following configuration:

Table 79. Delay Block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-	900	1300	1900	ps
t_{Δ}	Unit Delay	-	28	33	41	-

6.3.21 16-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 80*, *Table 81* and *Table 82* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 12: General operating conditions*.

Table 80. 16-bit ADC characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2$ V	1.62	-	V_{DDA}	V
		$V_{DDA} < 2$ V	V_{DDA}			V
V_{REF-}	Negative reference voltage	-	V_{SSA}			V

Table 80. 16-bit ADC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions				Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	1.62 V ≤ VDDA ≤ 3.6 V			BOOST = 11	0.12	-	50	MHz
					BOOST = 10	0.12	-	25	
					BOOST = 01	0.12	-	12.5	
					BOOST = 00	-	-	6.25	
f_s(3)	Sampling rate for Direct channels	Resolution = 16 bits, V_{DDA} >2.5 V	T_J = 90 °C	f_{ADC} = 36 MHz	SMP = 1.5	-	-	3.60	MSps
		Resolution = 16 bits		f_{ADC} = 37 MHz	SMP = 2.5	-	-	3.35	
		Resolution = 14 bits	T_J = 125 °C	f_{ADC} = 50 MHz	SMP = 2.5	-	-	5.00	
		Resolution = 12 bits		f_{ADC} = 50 MHz	SMP = 2.5	-	-	5.50	
		Resolution = 10 bits		f_{ADC} = 50 MHz	SMP = 1.5	-	-	7.10	
		Resolution = 8 bits		f_{ADC} = 50 MHz	SMP = 1.5	-	-	8.30	
		Resolution = 14 bits	T_J = 140 °C	f_{ADC} = 49 MHz	SMP = 1.5	-	-	4.90	
		Resolution = 12 bits		f_{ADC} = 50 MHz	SMP = 1.5	-	-	5.50	
		Resolution = 10 bits		f_{ADC} = 50 MHz	SMP = 1.5	-	-	6.70	
		Resolution = 8 bits		f_{ADC} = 50 MHz	SMP = 1.5	-	-	8.30	
	Sampling rate for Fast channels	Resolution = 16 bits, V_{DDA} >2.5 V	T_J = 90 °C	f_{ADC} = 32 MHz	SMP = 2.5	-	-	2.90	
		Resolution = 16 bits		f_{ADC} = 31 MHz	SMP = 2.5	-	-	2.80	
		Resolution = 14 bits	T_J = 125 °C	f_{ADC} = 33 MHz	SMP = 2.5	-	-	3.30	
		Resolution = 12 bits		f_{ADC} = 39 MHz	SMP = 2.5	-	-	4.30	
		Resolution = 10 bits		f_{ADC} = 48 MHz	SMP = 2.5	-	-	6.00	
		Resolution = 8 bits		f_{ADC} = 50 MHz	SMP = 2.5	-	-	7.10	
		Resolution = 12 bits	T_J = 140 °C	f_{ADC} = 37 MHz	SMP = 2.5	-	-	4.10	
		Resolution = 10 bits		f_{ADC} = 46 MHz	SMP = 2.5	-	-	5.70	
		Resolution = 8 bits		f_{ADC} = 50 MHz	SMP = 2.5	-	-	7.10	
	Sampling rate for Slow channels(4)	Resolution = 16 bits	T_J = 90 °C			-	-	1.00	
		resolution = 14 bits	T_J = 125 °C			-	-		
		resolution = 12 bits				-	-		
		resolution = 10 bits				-	-		
		resolution = 8 bits				-	-		
		resolution = 12 bits	T_J = 140 °C			-	-		
		resolution = 10 bits				-	-		
		resolution = 8 bits				-	-		
V_{AIN}(5)	Conversion voltage range	-				0	-	V_{REF+}	V
V_{CMIV}	Common mode input voltage	-				$V_{REF}/2$ − 10%	$V_{REF}/2$	$V_{REF}/2$ + 10%	V

Table 80. 16-bit ADC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
R_{AIN}(6)	External input impedance	Resolution = 16 bits, T_J = 125 °C	-	-	-	-	170	Ω
		Resolution = 14 bits, T_J = 125 °C	-	-	-	-	435	
		Resolution = 12 bits, T_J =125 °C	-	-	-	-	1,150	
		Resolution = 10 bits, T_J = 125 °C	-	-	-	-	5,650	
		Resolution = 8 bits, T_J = 125 °C	-	-	-	-	26,500	
C_{ADC}	Internal sample and hold capacitor	-			-	4	-	pF
$t_{ADCVREG\_STUP}$	ADC LDO startup time	-			-	5	10	us
t_{STAB}	ADC Power-up time	LDO already started			1	-	-	conver sion cycle
t_{CAL}	Offset and linearity calibration time	-			16,5010			$1/f_{ADC}$
t_{OFF_CAL}	Offset calibration time	-			1,280			$1/f_{ADC}$
t_{LATR}	Trigger conversion latency regular and injected channels without conversion abort	CKMODE = 00			1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01			-	-	2.5	
		CKMODE = 10			-	-	2.5	
		CKMODE = 11			-	-	2.25	
$t_{LATRINJ}$	Trigger conversion latency regular injected channels aborting a regular conversion	CKMODE = 00			2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01			-	-	3.5	
		CKMODE = 10			-	-	3.5	
		CKMODE = 11			-	-	3.25	
t_S	Sampling time	-			1.5	-	810.5	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	Resolution = N bits			ts + 0.5 + N/2	-	-	$1/f_{ADC}$
t_{TRIG}	External trigger period	-			t_{CONV}	-	-	$1/f_{ADC}$

Table 80. 16-bit ADC characteristics[(1)(2)] (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
I_{DDA_D} (ADC)	ADC consumption on V_{DDA}, BOOST=11, Differential mode	Resolution = 16 bits, f_{ADC} = 25 MHz	-	-	-	1,440	-	µA
		Resolution = 14 bits, f_{ADC} = 30 MHz	-	-	-	1,350	-	
		Resolution = 12 bits, f_{ADC} = 40 MHz	-	-	-	990	-	
	ADC consumption on V_{DDA}, BOOST=10, Differential mode, f_{ADC} = 25 MHz	Resolution = 16 bits	-	-	-	1,080	-	
		Resolution = 14 bits	-	-	-	810	-	
		Resolution = 12 bits	-	-	-	585	-	
	ADC consumption on V_{DDA}, BOOST=01, Differential mode, f_{ADC} = 12.5 MHz	Resolution = 16 bits	-	-	-	630	-	
		Resolution = 14 bits	-	-	-	432	-	
		Resolution = 12 bits	-	-	-	315	-	
	ADC consumption on V_{DDA}, BOOST=00, Differential mode, f_{ADC} = 6.25 MHz	Resolution = 16 bits	-	-	-	360	-	
		Resolution = 14 bits	-	-	-	270	-	
		Resolution = 12 bits	-	-	-	225	-	
I_{DDA_SE} (ADC)	ADC consumption on V_{DDA}, BOOST=11, Single-ended mode	Resolution = 16 bits, f_{ADC}=25 MHz	-	-	-	720	-	
		Resolution = 14 bits, f_{ADC}=30 MHz	-	-	-	675	-	
		Resolution = 12 bits, f_{ADC}=40 MHz	-	-	-	495	-	
	ADC consumption on V_{DDA}, BOOST=10, Singl-ended mode, f_{ADC} = 25 MHz	Resolution = 16 bits	-	-	-	540	-	
		Resolution = 14 bits	-	-	-	405	-	
		Resolution = 12 bits	-	-	-	292.5	-	
	ADC consumption on V_{DDA}, BOOST=01, Single-ended mode, f_{ADC} = 12.5 MHz	Resolution = 16 bits	-	-	-	315	-	
		Resolution = 14 bits	-	-	-	216	-	
		Resolution = 12 bits	-	-	-	157.5	-	
	ADC consumption on V_{DDA} BOOST=00, Single-ended mode f_{ADC}=6.25 MHz	Resolution = 16 bits	-	-	-	180	-	
		Resolution = 14 bits	-	-	-	135	-	
		Resolution = 12 bits	-	-	-	112.5	-	
I_{DD} (ADC)	ADC consumption on V_{DD}	f_{ADC}=50 MHz	-	-	-	400	-	
		f_{ADC}=25 MHz	-	-	-	220	-	
		f_{ADC}=12.5 MHz	-	-	-	180	-	
		f_{ADC}=6.25 MHz	-	-	-	120	-	
		f_{ADC}=3.125 MHz	-	-	-	80	-	

1. Guaranteed by design.
2. The voltage booster on ADC switches must be used for V_{DDA} < 2.4 V (embedded I/O switches).
3. These values are valid for TFBGA100, UFBGA169 and UFBGA176+25 packages and one ADC. The values for other packages and multiple ADCs may be different.
4. For slow channels, the performance should be limited to 1 Msps what ever the value of f_{ADC}.

5. Depending on the package, V_{REF+} can be internally connected to V_{DDA} and V_{REF-} to V_{SSA}.
6. The tolerance is 10 LSBs for 16-bit resolution, 4 LSBs for 14-bit resolution, and 2 LSBs for 12-bit, 10-bit and 8-bit resolutions.

Table 81. Minimum sampling time vs R_{AIN} (16-bit ADC)(1)(2)

Resolution	RAIN (Ω)	Minimum sampling time (s)		
		Direct channels(3)	Fast channels(4)	Slow channels(5)
16 bits	47	7.37E-08	1.14E-07	1.72E-07
14 bits	47	6.29E-08	9.74E-08	1.55E-07
	68	6.84E-08	1.02E-07	1.58E-07
	100	7.80E-08	1.12E-07	1.62E-07
	150	9.86E-08	1.32E-07	1.80E-07
	220	1.32E-07	1.61E-07	2.01E-07
12 bits	47	5.32E-08	8.00E-08	1.29E-07
	68	5.74E-08	8.50E-08	1.32E-07
	100	6.58E-08	9.31E-08	1.40E-07
	150	8.37E-08	1.10E-07	1.51E-07
	220	1.11E-07	1.34E-07	1.73E-07
	330	1.56E-07	1.78E-07	2.14E-07
	470	2.16E-07	2.39E-07	2.68E-07
	680	3.01E-07	3.29E-07	3.54E-07
10 bits	47	4.34E-08	6.51E-08	1.08E-07
	68	4.68E-08	6.89E-08	1.11E-07
	100	5.35E-08	7.55E-08	1.16E-07
	150	6.68E-08	8.77E-08	1.26E-07
	220	8.80E-08	1.08E-07	1.40E-07
	330	1.24E-07	1.43E-07	1.71E-07
	470	1.69E-07	1.89E-07	2.13E-07
	680	2.38E-07	2.60E-07	2.80E-07
	1000	3.45E-07	3.66E-07	3.84E-07
	1500	5.15E-07	5.35E-07	5.48E-07
	2200	7.42E-07	7.75E-07	7.78E-07
	3300	1.10E-06	1.14E-06	1.14E-06

Table 81. Minimum sampling time vs R_{AIN} (16-bit ADC)(1)(2) (continued)

Resolution	RAIN (Ω)	Minimum sampling time (s)		
		Direct channels(3)	Fast channels(4)	Slow channels(5)
8 bits	47	3.32E-08	5.10E-08	8.61E-08
	68	3.59E-08	5.35E-08	8.83E-08
	100	4.10E-08	5.83E-08	9.22E-08
	150	5.06E-08	6.76E-08	9.95E-08
	220	6.61E-08	8.22E-08	1.11E-07
	330	9.17E-08	1.08E-07	1.32E-07
	470	1.24E-07	1.40E-07	1.63E-07
	680	1.74E-07	1.91E-07	2.12E-07
	1000	2.53E-07	2.70E-07	2.85E-07
	1500	3.73E-07	3.93E-07	4.05E-07
	2200	5.39E-07	5.67E-07	5.75E-07
	3300	8.02E-07	8.36E-07	8.38E-07
	4700	1.13E-06	1.18E-06	1.18E-06
	6800	1.62E-06	1.69E-06	1.68E-06
	10000	2.36E-06	2.47E-06	2.45E-06
	15000	3.50E-06	3.69E-06	3.65E-06

1. Guaranteed by design.
2. Data valid at up to 130 °C, with a 47 pF PCB capacitor, and V_{DDA}=1.6 V.
3. Direct channels are connected to analog I/Os (PA0_C, PA1_C, PC2_C and PC3_C) to optimize ADC performance.
4. Fast channels correspond to PA6, PB1, PC4, PF11, PF13 for ADCx_INPx, and to PA7, PB0, PC5, PF12, PF14 for ADCx_INNx.
5. Slow channels correspond to all ADC inputs except for the Direct and Fast channels.

Table 82. 16-bit ADC accuracy(1)(2)

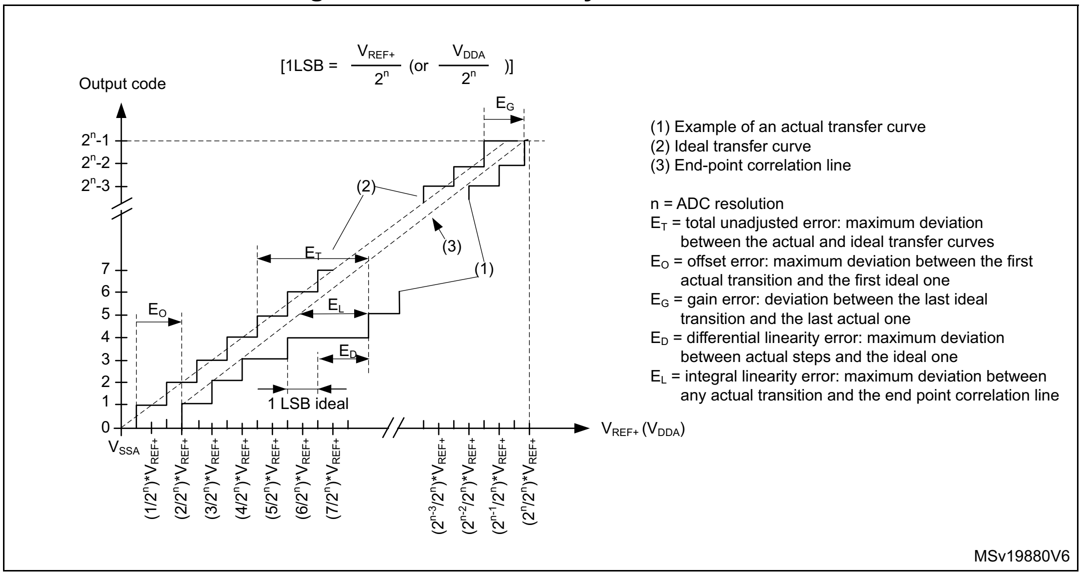
Symbol	Parameter	Conditions(3)		Min	Typ	Max	Unit
ET	Total undadjusted error	Direct channel	Single ended	-	+10/–20	-	LSB
			Differential	-	±15	-	
		Fast channel	Single ended	-	+10/–20	-	
			Differential	-	±15	-	
		Slow channel	Single ended	-	±10	-	
			Differential		±10	-	
EO	Offset error	-		-	±10	-	
EG	Gain error	-		-	±15	-	
ED	Differential linearity error	Single ended		-	+3/–1	-	
		Differential		-	+4.5/–1	-	
EL	Integral linearity error	Direct channel	Single ended	-	±11	-	
			Differential	-	±7	-	
		Fast channel	Single ended	-	±13	-	
			Differential	-	±7	-	
		Slow channel	Single ended	-	±10	-	
			Differential	-	±6	-	
ENOB	Effective number of bits	Single ended		-	12.2	-	Bits
		Differential		-	13.2	-	
SINAD	Signal-to-noise and distortion ratio	Single ended		-	75.2	-	dB
		Differential		-	81.2	-	
SNR	Signal-to-noise ratio	Single ended		-	77.0	-	
		Differential		-	81.0	-	
THD	Total harmonic distortion	Single ended		-	87	-	
		Differential		-	90	-	

1. Guaranteed by characterization results for BGA packages. The values for LQFP packages might differ.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC clock frequency = 25 MHz, ADC resolution = 16 bits, V_{DDA}=V_{REF+}=3.3 V, BOOST=11 and 16-bit mode.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

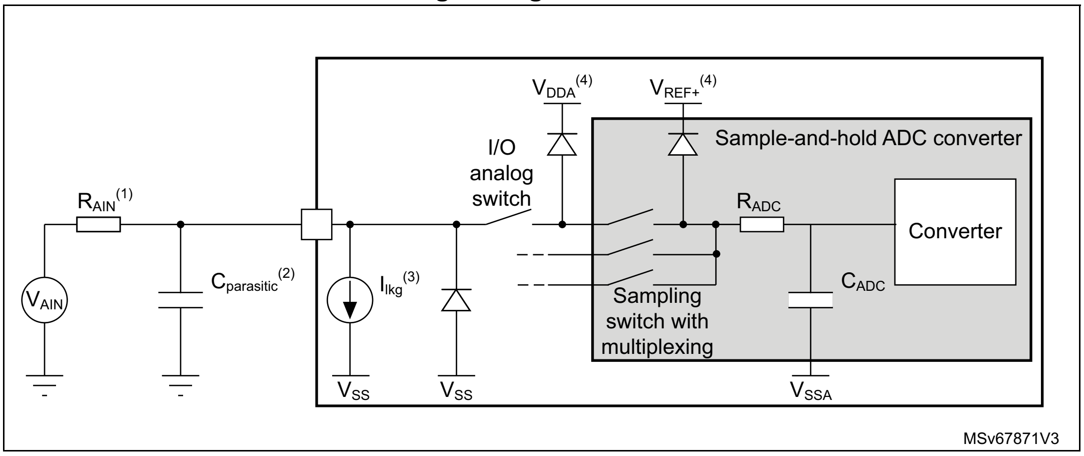
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ does not affect the ADC accuracy.

Figure 35. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 36. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function

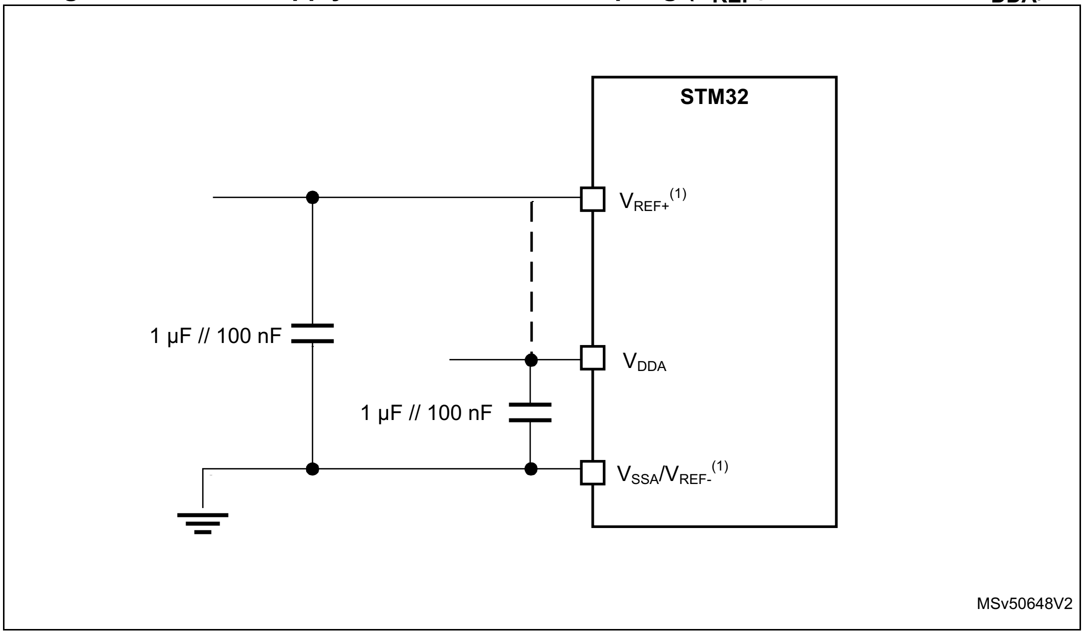


1. Refer to *Table 80: 16-bit ADC characteristics* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 51: I/O static characteristics*). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 51: I/O static characteristics* for the value of I_{lkg}.
4. Refer to *Figure 10: Power supply scheme*.

General PCB design guidelines

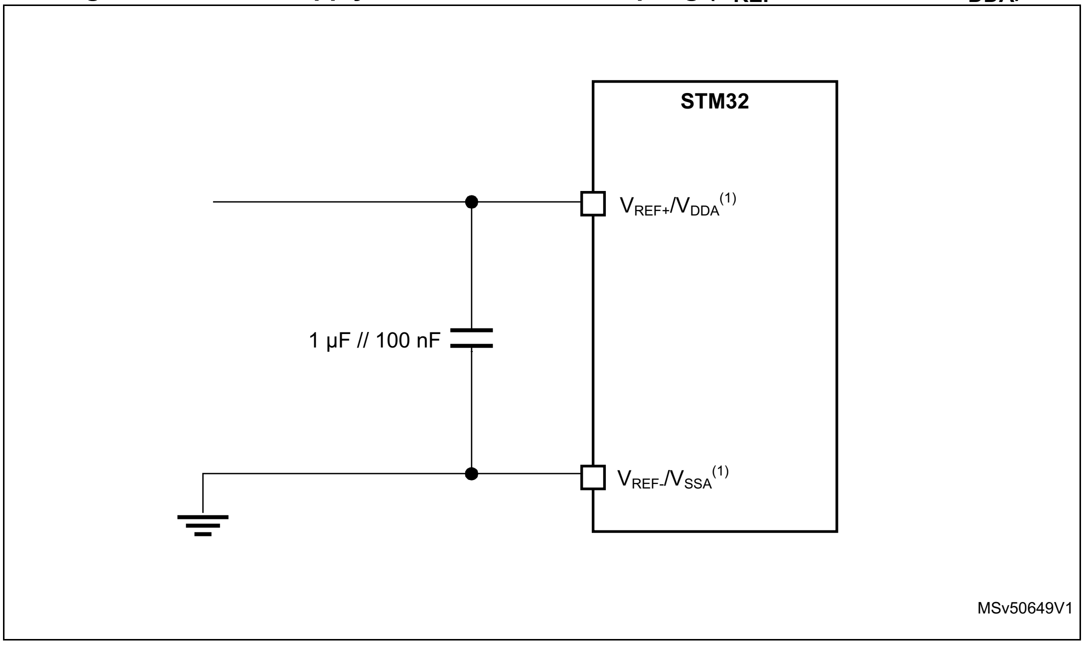
Power supply decoupling should be performed as shown in *Figure 37* or *Figure 38*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 100 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 37. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. When V_{REF+} and V_{REF-} inputs are not available, they are internally connected to V_{DDA} and V_{SSA}, respectively.

Figure 38. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. When V_{REF+} and V_{REF-} inputs are not available, they are internally connected to V_{DDA} and V_{SSA}, respectively.

6.3.22 12-bit ADC characteristics

Unless otherwise specified, the parameters given in Table 83, Table 84 and Table 85 are derived from tests performed under the ambient temperature and V_{DDA} supply voltage conditions summarized in Table 12: General operating conditions. In Table 83, Table 84 and Table 85, f_{ADC} refers to $f_{adc\_ker\_ck}$.

Table 83. 12-bit ADC characteristics(1)(2)

<table>
<tr><th>Sym-bol</th><th>Parameter</th><th colspan="6">Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>V_{DDA}</td><td>Analog power supply for ADC ON</td><td colspan="6">-</td><td>1.62</td><td>-</td><td>3.6</td><td rowspan="3">V</td></tr>
<tr><td>V_{REF+}(3)</td><td>Positive reference voltage</td><td colspan="6">$V_{DDA} \geq V_{REF+}$</td><td>1.62</td><td>-</td><td>V_{DDA}</td></tr>
<tr><td>V_{REF-}</td><td>Negative reference voltage</td><td colspan="6">-</td><td>V_{SSA}</td><td>-</td><td>-</td></tr>
<tr><td>f_{ADC}</td><td>ADC clock frequency</td><td colspan="6">1,62 V ≤ V_{DDA} ≤ 3.6 V</td><td>1.5</td><td>-</td><td>75</td><td>MHz</td></tr>
<tr><td rowspan="16">f_S(4)</td><td rowspan="16">Sampling rate for Direct channels</td><td rowspan="4">Resolution = 12 bits</td><td rowspan="2">Continuous and Discontinuous mode(5)</td><td>2.4 V ≤ V_{DDA} ≤ 3.6 V</td><td rowspan="4">–40 °C ≤ T_J ≤ 130 °C</td><td>f_{ADC} = 75 MHz</td><td rowspan="4">SMP = 2.5</td><td>-</td><td>-</td><td>5</td><td rowspan="16">MSPS</td></tr>
<tr><td>1.6V ≤ V_{DDA} ≤ 3.6 V</td><td>f_{ADC} = 60 MHz</td><td>-</td><td>-</td><td>4</td></tr>
<tr><td rowspan="2">Single mode</td><td>2.4 V ≤ V_{DDA} ≤ 3.6 V</td><td>f_{ADC} = 50 MHz(6)</td><td>-</td><td>-</td><td>3.33</td></tr>
<tr><td>1.6 V ≤ V_{DDA} ≤ 3.6 V</td><td>f_{ADC} = 38 MHz(6)</td><td>-</td><td>-</td><td>2.53</td></tr>
<tr><td rowspan="3">Resolution = 10 bits</td><td>Continuous and Discontinuous mode(5)</td><td>1.6V ≤ V_{DDA} ≤ 3.6V</td><td rowspan="3">–40 °C ≤ T_J ≤ 130 °C</td><td>f_{ADC} = 75 MHz</td><td rowspan="3">SMP = 2.5</td><td>-</td><td>-</td><td>5.77</td></tr>
<tr><td rowspan="2">Single mode</td><td>2.4 V ≤ V_{DDA} ≤ 3.6 V</td><td>f_{ADC} = 58 MHz(6)</td><td>-</td><td>-</td><td>4.46</td></tr>
<tr><td>1.6V ≤ V_{DDA} ≤ 3.6V</td><td>f_{ADC} = 42 MHz(6)</td><td>-</td><td>-</td><td>3.23</td></tr>
<tr><td rowspan="3">Resolution = 8 bits</td><td>Continuous and Discontinuous mode(5)</td><td>1.6V ≤ V_{DDA} ≤ 3.6V</td><td rowspan="3">–40 °C ≤ T_J ≤ 130 °C</td><td>f_{ADC} = 75 MHz</td><td rowspan="3">SMP = 2.5</td><td>-</td><td>-</td><td>6.82</td></tr>
<tr><td rowspan="2">Single mode</td><td>2.4 V ≤ V_{DDA} ≤ 3.6 V</td><td>f_{ADC} = 67 MHz(6)</td><td>-</td><td>-</td><td>6.09</td></tr>
<tr><td>1.6V ≤ V_{DDA} ≤ 3.6V</td><td>f_{ADC} = 48 MHz(6)</td><td>-</td><td>-</td><td>4.36</td></tr>
<tr><td rowspan="3">Resolution = 6 bits</td><td>Continuous and Discontinuous mode(5)</td><td>1.6V ≤ V_{DDA} ≤ 3.6V</td><td rowspan="3">–40 °C ≤ T_J ≤ 130 °C</td><td>f_{ADC} = 75 MHz</td><td rowspan="3">SMP = 2.5</td><td>-</td><td>-</td><td>8.33</td></tr>
<tr><td rowspan="2">Single mode</td><td>2.4 V ≤ V_{DDA} ≤ 3.6 V</td><td>f_{ADC} = 75 MHz(6)</td><td>-</td><td>-</td><td>8.33</td></tr>
<tr><td>1.6V ≤ V_{DDA} ≤ 3.6V</td><td>f_{ADC} = 55 MHz(6)</td><td>-</td><td>-</td><td>6.11</td></tr>
</table>

Table 83. 12-bit ADC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions						Min	Typ	Max	Unit
f_S(4) (continued)	Sampling rate for fast channels (VIN[0:5])	Resolution = 12 bits	Continuous and Discontinuous mode(5)	$2.4\ V \le V_{DDA} \le 3.6\ V$	$-40\ °C \le T_J \le 130\ °C$	f_{ADC} = 65 MHz	SMP = 2.5	-	-	4.33	MSPS
				$1.6V \le V_{DDA} \le 3.6V$		f_{ADC} = 58 MHz		-	-	3.87	
			Single mode	$2.4\ V \le V_{DDA} \le 3.6\ V$		f_{ADC} = 32 MHz(6)		-	-	2.13	
				$1.6V \le V_{DDA} \le 3.6V$		f_{ADC} = 26 MHz(6)		-	-	1.73	
		Resolution = 10 bits	Continuous and Discontinuous mode(5)	$1.6V \le V_{DDA} \le 3.6V$	$-40\ °C \le T_J \le 130\ °C$	f_{ADC} = 75 MHz	SMP = 2.5	-	-	5.77	
			Single mode	$2.4\ V \le V_{DDA} \le 3.6\ V$		f_{ADC} = 36 MHz(6)		-	-	2.77	
				$1.6V \le V_{DDA} \le 3.6V$		f_{ADC} = 30 MHz(6)		-	-	2.31	
		Resolution = 8 bits	Continuous and Discontinuous mode(5)	$1.6V \le V_{DDA} \le 3.6V$	$-40\ °C \le T_J \le 130\ °C$	f_{ADC} = 75 MHz	SMP = 2.5	-	-	6.82	
			Single mode	$2.4\ V \le V_{DDA} \le 3.6\ V$		f_{ADC} =44 MHz(6)		-	-	4.00	
				$1.6V \le V_{DDA} \le 3.6V$		f_{ADC} = 35 MHz(6)		-	-	3.18	
		Resolution = 6 bits	Continuous and Discontinuous mode(5)	$1.6V \le V_{DDA} \le 3.6V$	$-40\ °C \le T_J \le 130\ °C$	f_{ADC} = 75 MHz	SMP = 2.5	-	-	8.33	
			Single mode	$2.4\ V \le V_{DDA} \le 3.6\ V$		f_{ADC} = 56 MHz(6)		-	-	6.22	
				$1.6V \le V_{DDA} \le 3.6V$		f_{ADC} = 42 MHz(6)		-	-	4.66	
	Sampling rate for slow channels	Resolution = 12 bits	-	-	$-40\ °C \le T_J \le 130\ °C$	f_{ADC} = 15 MHz(6)	SMP = 2.5	-	-	1.00	
		Resolution = 10 bits						-	-	1.28	
		Resolution = 8 bits						-	-	1.63	
		Resolution = 6 bits						-	-	2.08	
t_{TRIG}	External trigger period	Resolution = 12 bits						-	-	15	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-						0	-	V_{REF+}	V
V_{CMIV}	Common mode input voltage	-						$V_{REF}/2-10\%$	$V_{REF}/2$	$V_{REF}/2 + 10\%$	
R_{AIN}(7)	External input impedance	Resolution = 12 bits, T_J = 125 °C						-	-	220	Ω
		Resolution = 10 bits, T_J = 125 °C						-	-	2100	
		Resolution = 8 bits, T_J = 125 °C						-	-	12000	
		Resolution = 6 bits, T_J = 125 °C						-	-	80000	

Table 83. 12-bit ADC characteristics(1)(2) (continued)

Sym-bol	Parameter	Conditions	Min	Typ	Max	Unit
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
$t_{ADCVREG\_STUP}$	ADC LDO startup time	-	-	5	10	µs
t_{STAB}	ADC power-up time	LDO already started	1	-	-	con-version cycle
t_{OFF_CAL}	Offset calibration time	-	135	-	-	$1/f_{ADC}$
t_{LATR}	Trigger conversion latency for regular and injected channels without aborting the conversion	CKMODE = 00	1.5	2	2.5	
		CKMODE = 01	-	-	2.5	
		CKMODE = 10	-	-	2.5	
		CKMODE = 11	-	-	2.25	
$t_{LATRINJ}$	Trigger conversion latency for regular and injected channels when a regular conversion is aborted	CKMODE = 00	2.5	3	3.5	
		CKMODE = 01	-	-	3.5	
		CKMODE = 10	-	-	3.5	
		CKMODE = 11	-	-	3.25	
t_S	Sampling time	-	2.5	-	640.5	
t_{CONV}	Total conversion time (including sampling time)	N-bits resolution	t_S + 0.5 + N	-	-	
$I_{DDA\_D(ADC)}$	ADC consumption on V_{DDA} and V_{REF}, Differential mode	f_S= 5 MSPS	-	430	-	µA
		f_S = 1 MSPS	-	133	-	
		f_S = 0.1 MSPS	-	51	-	
$I_{DDA\_SE(ADC)}$	ADC consumption on V_{DDA} and V_{REF}, Single-ended mode	f_S= 5 MSPS	-	350	-	
		f_S = 1 MSPS	-	122	-	
		f_S = 0.1 MSPS	-	47	-	
$I_{DD(ADC)}$	ADC consumption on V_{DD} per f_{ADC}	-	-	2.4	-	µA/MHz

1. Guaranteed by design.
2. The voltage booster on ADC switches must be used for V_{DDA} < 2.4 V (embedded I/O switches).
3. Depending on the package, VREF+ can be internally connected to V_{DDA} and VREF- to V_{SSA}.
4. Guaranteed by characterization for BGA and CSP packages. The values for LQFP packages may be different.
5. The conversion of the first element in the group is excluded.

6. f_{ADC} value corresponds to the maximum frequency that can be reached considering a 2.5 sampling period. For other SMPy sampling periods, the maximum frequency is f_{ADC} value * SMPy / 2.5 with a limitation to 75 MHz.
7. The tolerance is 2 LSBs for 12-bit, 10-bit and 8-bit resolutions. It is otherwise specified.

Table 84. Minimum sampling time vs R_{AIN} (12-bit ADC)(1)(2)

Resolution	R_{AIN} (Ω)	Minimum sampling time (s)		
		Direct channels(3)	Fast channels(4)	Slow channels(5)
12 bits	47	5.55E-08	7.04E-08	1.03E-07
	68	5.76E-08	7.22E-08	1.05E-07
	100	6.17E-08	7.65E-08	1.07E-07
	150	7.02E-08	8.45E-08	1.13E-07
	220	8.59E-08	1.00E-07	1.22E-07
	330	1.11E-07	1.26E-07	1.41E-07
	470	1.46E-07	1.61E-07	1.69E-07
	680	1.98E-07	2.17E-07	2.25E-07
10 bits	47	4.90E-08	6.06E-08	8.77E-08
	68	5.07E-08	6.27E-08	8.95E-08
	100	5.41E-08	6.67E-08	9.22E-08
	150	6.18E-08	7.50E-08	9.59E-08
	220	7.51E-08	8.70E-08	1.04E-07
	330	9.46E-08	1.07E-07	1.17E-07
	470	1.22E-07	1.34E-07	1.42E-07
	680	1.63E-07	1.77E-07	1.86E-07
	1000	2.27E-07	2.42E-07	2.43E-07
	1500	3.27E-07	3.40E-07	3.35E-07
	2200	4.53E-07	4.86E-07	4.73E-07
	3300	6.56E-07	6.93E-07	6.72E-07

Table 84. Minimum sampling time vs R_{AIN} (12-bit ADC)[1][2] (continued)

Resolution	R_{AIN} (Ω)	Minimum sampling time (s)		
		Direct channels[3]	Fast channels[4]	Slow channels[5]
8 bits	47	4.35E-08	5.31E-08	7.36E-08
	68	4.47E-08	5.48E-08	7.47E-08
	100	4.72E-08	5.79E-08	7.63E-08
	150	5.33E-08	6.35E-08	7.88E-08
	220	6.26E-08	7.26E-08	8.47E-08
	330	7.84E-08	8.80E-08	9.48E-08
	470	9.80E-08	1.07E-07	1.14E-07
	680	1.28E-07	1.39E-07	1.43E-07
	1000	1.76E-07	1.88E-07	1.90E-07
	1500	2.49E-07	2.66E-07	2.64E-07
	2200	3.50E-07	3.63E-07	3.63E-07
	3300	5.09E-07	5.27E-07	5.24E-07
	4700	7.00E-07	7.28E-07	7.09E-07
	6800	9.84E-07	1.03E-06	1.00E-06
	10000	1.43E-06	1.48E-06	1.44E-06
	15000	2.10E-06	2.18E-06	2.11E-06
6 bits	47	3.79E-08	4.58E-08	5.74E-08
	68	3.88E-08	4.69E-08	5.81E-08
	100	4.09E-08	4.89E-08	5.93E-08
	150	4.48E-08	5.25E-08	6.14E-08
	220	5.07E-08	5.81E-08	6.58E-08
	330	6.04E-08	6.79E-08	7.46E-08
	470	7.37E-08	8.10E-08	8.60E-08
	680	9.31E-08	1.01E-07	1.04E-07
	1000	1.23E-07	1.32E-07	1.34E-07
	1500	1.71E-07	1.82E-07	1.82E-07
	2200	2.39E-07	2.50E-07	2.49E-07
	3300	3.43E-07	3.57E-07	3.49E-07
	4700	4.72E-07	4.92E-07	4.81E-07
	6800	6.65E-07	6.89E-07	6.68E-07
	10000	9.54E-07	9.88E-07	9.54E-07
	15000	1.40E-06	1.45E-06	1.39E-06

1. Guaranteed by design.
2. Data valid up to 130 °C, with a 22 pF PCB capacitor and V_{DDA} = 1.62 V.

3. Direct channels are connected to analog I/Os (PA0_C, PA1_C, PC2_C and PC3_C) to optimize ADC performance.
4. Fast channels correspond to ADCx_INx[0:5].
5. Slow channels correspond to all ADC inputs except for the Direct and Fast channels.

Table 85. 12-bit ADC accuracy(1)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ET	Total unadjusted error	Direct channel	Single ended	-	3.5	5	±LSB
			Differential	-	2.5	3	
		Fast channel	Single ended	-	3.5	5	
			Differential	-	2.5	3	
		Slow channel	Single ended	-	3.5	5	
			Differential	-	2.5	3	
EO	Offset error	-		-	+/-2	+/-5	
EG	Gain error	-		-	TBD (3)	-	
ED	Differential linearity error	Single ended		-	+/-0.75	+1.5/-1	
		Differential		-	+/-0.5	+1.25/-1	
EL	Integral linearity error	Direct channel	Single ended	-	+/-1	+/-2.5	
			Differential	-	+/-1	+/-2	
		Fast channel	Single ended	-	+/-1	+/-2.5	
			Differential	-	+/-1	+/-2	
		Slow channel	Single ended	-	+/-1	+/-2.5	
			Differential	-	+/-1	+/-2	
ENOB	Effective number of bits	Single ended		-	11.2	-	bits
		Differential		-	11.5	-	
SINAD	Signal-to-noise and distortion ratio	Single ended		-	68.9	-	dB
		Differential		-	71.1	-	
SNR	Signal-to-noise ratio	Single ended		-	69.1	-	
		Differential		-	71.4	-	
THD	Total harmonic distortion	Single ended		-	-79.6	-	
		Differential		-	-81.8	-	

1. Guaranteed by characterization for BGA packages. The maximum values are preliminary data. The values for LQFP packages may be different.
2. ADC DC accuracy values are measured after internal calibration in Continuous and Discontinuous mode.
3. TBD stands for “to be defined”.

6.3.23 DAC characteristics

Table 86. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.8	3.3	3.6	V
V_{REF+}	Positive reference voltage	-		1.80	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-		-	V_{SSA}	-	V
R_L	Resistive Load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	kΩ
R_O	Output Impedance	DAC output buffer OFF		10.3	13	16	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON	V_{DD} = 2.7 V	-	-	1.6	kΩ
			V_{DD} = 2.0 V	-	-	2.6	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF	V_{DD} = 2.7 V	-	-	17.8	kΩ
			V_{DD} = 2.0 V	-	-	18.7	
C_L	Capacitive Load	DAC output buffer OFF		-	-	50	pF
C_{SH}		Sample and Hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{REF+} − 0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ±0.5LSB, ±1LSB, ±2LSB, ±4LSB, ±8LSB)	Normal mode, DAC output buffer ON, $C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ	±0.5 LSB	-	2.05	3	µs
			±1 LSB	-	1.97	2.87	
			±2 LSB	-	1.67	2.84	
			±4 LSB	-	1.66	2.78	
			±8 LSB	-	1.65	2.7	
		Normal mode, DAC output buffer OFF, ±1LSB C_L=10 pF		-	1.7	2	
t_{WAKEUP}(2)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until the final value of ±1LSB is reached	Normal mode, DAC output buffer ON, $C_L \leq$ 50 pF, R_L = 5 kΩ		-	5	7.5	µs
		Normal mode, DAC output buffer OFF, $C_L \leq$ 10 pF			2	5	
PSRR	DC V_{DDA} supply rejection ratio	Normal mode, DAC output buffer ON, $C_L \leq$ 50 pF, R_L = 5 kΩ		-	−80	−28	dB

Table 86. DAC characteristics[(1)] (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{SAMP}	Sampling time in Sample and Hold mode C_L=100 nF (code transition between the lowest input code and the highest input code when DAC_OUT reaches the ±1LSB final value)	MODE<2:0>_V12=100/101 (BUFFER ON)		-	0.7	2.6	ms
		MODE<2:0>_V12=110 (BUFFER OFF)		-	11.5	18.7	ms
		MODE<2:0>_V12=111 (INTERNAL BUFFER OFF)		-	0.3	0.6	µs
I_{leak}	Output leakage current	-			(3)		nA
C_{Iint}	Internal sample and hold capacitor	-		1.8	2.2	2.6	pF
t_{TRIM}	Middle code offset trim time	Minimum time to verify the each code		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	850	-	µV
		V_{REF+} = 1.8 V		-	425	-	µV
$I_{DDA(DAC)}$	DAC quiescent consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	360	-	µA
			No load, worst code (0xF1C)	-	490	-	µA
		DAC output buffer OFF	No load, middle/ worst code (0x800)	-	20	-	µA
		Sample and Hold mode, C_{SH}=100 nF		-	$360*T_{ON}/(T_{ON}+T_{OFF})$ (4)	-	µA
$I_{DDV}(DAC)$	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	170	-	µA
			No load, worst code (0xF1C)	-	170	-	µA
		DAC output buffer OFF	No load, middle/ worst code (0x800)	-	160	-	µA
		Sample and Hold mode, Buffer ON, C_{SH}=100 nF (worst code)		-	$170*T_{ON}/(T_{ON}+T_{OFF})$ (4)	-	µA
		Sample and Hold mode, Buffer OFF, C_{SH}=100 nF (worst code)		-	$160*T_{ON}/(T_{ON}+T_{OFF})$ (4)	-	µA

1. Guaranteed by design unless otherwise specified.

2. In buffered mode, the output can overshoot above the final value for low input code (starting from the minimum value).
3. Refer to *Table 51: I/O static characteristics*.
4. T_{ON} is the refresh phase duration, while T_{OFF} is the hold phase duration. Refer to the product reference manual for more details.

Table 87. DAC accuracy(1)

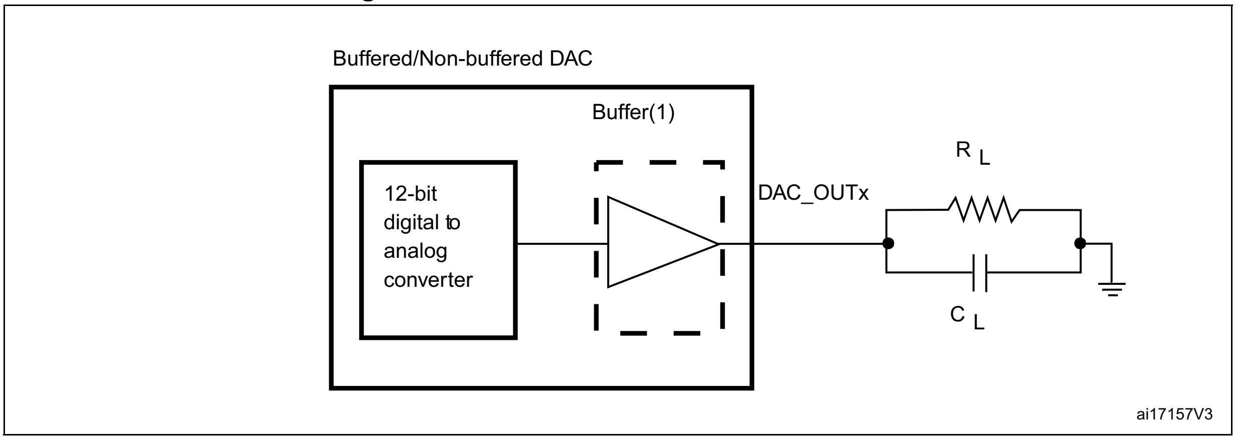
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DNL	Differential non linearity(2)	DAC output buffer ON	−2	-	2	LSB
		DAC output buffer OFF	−2	-	2	
-	Monotonicity	10 bits	-	-	-	-
INL	Integral non linearity(3)	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ	−4	-	4	LSB
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L	−4	-	4	
Offset	Offset error at code 0x800 (3)	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ, V_{REF+} = 3.6 V	-	-	±12	LSB
		DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ, V_{REF+} = 1.8 V	-	-	±25	
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L	-	-	±8	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF, $C_L \leq 50$ pF, no R_L	-	-	±5	LSB
OffsetCal	Offset error at code 0x800 after factory calibration	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ, V_{REF+} = 3.6 V	-	-	±5	LSB
		DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ, V_{REF+} = 1.8 V	-	-	±7	
Gain	Gain error(5)	DAC output buffer ON,$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-	±1	%
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L	-	-	±1	
TUE	Total unadjusted error	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-	±30	LSB
		DAC output buffer OFF, $C_L \leq$ 50 pF, no R_L			±12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-	±23	
SNR	Signal-to-noise ratio(6)	DAC output buffer ON,$C_L \leq 50$ pF, $R_L \geq 5$ kΩ , 1 kHz, BW = 500 KHz	-	67.8	-	dB
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L,1 kHz, BW = 500 KHz	-	67.8	-	

Table 87. DAC accuracy[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	Total harmonic distortion[6]	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ , 1 kHz	-	−78.6	-	dB
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L, 1 kHz	-	−78.6	-	
SINAD	Signal-to-noise and distortion ratio[6]	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ , 1 kHz	-	67.5	-	dB
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L, 1 kHz	-	67.5	-	
ENOB	Effective number of bits	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ , 1 kHz	-	10.9	-	bits
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L, 1 kHz	-	10.9	-	

1. Guaranteed by characterization results.
2. Difference between two consecutive codes minus 1 LSB.
3. Difference between the value measured at Code i and the value measured at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between the ideal slope of the transfer function and the measured slope computed from code 0x000 and 0xFFF when the buffer is OFF, and from code giving 0.2 V and (V_{REF+} - 0.2 V) when the buffer is ON.
6. Signal is −0.5dBFS with $F_{sampling}$=1 MHz.

Figure 39. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.24 Voltage reference buffer characteristics

Table 88. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode, V_{DDA} = 3.3 V	VSCALE = 000	2.8	3.3	3.6	V
			VSCALE = 001	2.4	-	3.6	
			VSCALE = 010	2.1	-	3.6	
			VSCALE = 011	1.8	-	3.6	
		Degraded mode(2)	VSCALE = 000	1.62	-	2.80	
			VSCALE = 001	1.62	-	2.40	
			VSCALE = 010	1.62	-	2.10	
			VSCALE = 011	1.62	-	1.80	
V_{REFBUF_OUT}	Voltage Reference Buffer Output, at 30 °C, I_{load}= 100 µA	Normal mode at 30 °C, I_{load} = 100 µA	VSCALE = 000	2.4980	2.5000	2.5035	
			VSCALE = 001	2.0460	2.0490	2.0520	
			VSCALE = 010	1.8010	1.8040	1.8060	
			VSCALE = 011	1.4995	1.5015	1.5040	
		Degraded mode(2)	VSCALE = 000	V_{DDA}− 150 mV	-	V_{DDA}	
			VSCALE = 001	V_{DDA}− 150 mV	-	V_{DDA}	
			VSCALE = 010	V_{DDA}− 150 mV	-	V_{DDA}	
			VSCALE = 011	V_{DDA}− 150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
C_L	Load capacitor	-	-	0.5	1	1.50	µF
esr	Equivalent Serial Resistor of C_L	-	-	-	-	2	Ω
I_{LOAD}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	-	ppm/V
			I_{load} = 4 mA	-	100	-	
I_{load_reg}	Load regulation	500 µA ≤ I_{LOAD} ≤ 4 mA	Normal mode	-	50	-	ppm/ mA
T_{coeff}	Temperature coefficient	−40 °C < T_J < +130 °C		-	-	T_{coeff} V_{REFINT} + 100	ppm/ °C
PSRR	Power supply rejection	DC	-	-	60	-	dB
		100KHz	-	-	40	-	

Table 88. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{START}	Start-up time	C_L=0.5 µF	-	-	300	-	µs
		C_L=1 µF	-	-	500	-	
		C_L=1.5 µF	-	-	650	-	
I_{INRUSH}	Control of maximum DC current drive on V_{REFBUF_OUT} during startup phase(3)	-		-	8	-	mA
I_{DDA} (VREFBUF)	VREFBUF consumption from V_{DDA}	I_{LOAD} = 0 µA	-	-	15	25	µA
		I_{LOAD} = 500 µA	-	-	16	30	
		I_{LOAD} = 4 mA	-	-	32	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer cannot accurately maintain the output voltage (V_{DDA}−drop voltage).
3. To properly control VREFBUF I_{INRUSH} current during the startup phase and the change of scaling, V_{DDA} voltage should be in the range of 1.8 V-3.6 V, 2.1 V-3.6 V, 2.4 V-3.6 V and 2.8 V-3.6 V for VSCALE = 011, 010, 001 and 000, respectively.

6.3.25 Analog temperature sensor characteristics

Table 89. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	-	±3	°C
Avg_Slope(2)	Average slope	-	2	-	mV/°C
V_{30}(3)	Voltage at 30°C ± 5 °C	-	0.62	-	V
t_{start_run}	Startup time in Run mode (buffer startup)	-	-	25.2	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	9	-	-	
I_{sens}(1)	Sensor consumption	-	0.18	0.31	µA
$I_{sensbuf}$(1)	Sensor buffer consumption	-	3.8	6.5	

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte.

Table 90. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 30 °C, V_{DDA}=3.3 V	0x1FF1 E820 -0x1FF1 E821
TS_CAL2	Temperature sensor raw data acquired value at 130 °C, V_{DDA}=3.3 V	0x1FF1 E840 - 0x1FF1 E841

6.3.26 Digital temperature sensor characteristics

Table 91. Digital temperature sensor characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DTS}(2)	Output Clock frequency	-	500	750	1150	kHz
T_{LC}(2)	Temperature linearity coefficient	VOS2	1660	2100	2750	Hz/°C
T_{TOTAL_ERROR}(2)	Temperature offset measurement, all VOS	T_J = −40°C to 30°C	−13	-	4	°C
		T_J = 30°C to Tjmax	−7	-	2	
T_{VDD_CORE}	Additional error due to supply variation	VOS2	0	-	0	°C
		VOS0, VOS1, VOS3	−1	-	1	
t_{TRIM}	Calibration time	-	-	-	2	ms
t_{WAKE_UP}	Wake-up time from off state until DTS ready bit is set	-	-	67	116.00	µs
I_{DDCORE_DTS}	DTS consumption on VDD_CORE	-	8.5	30	70.0	µA

1. Guaranteed by design, unless otherwise specified.
2. Guaranteed by characterization results.

6.3.27 Temperature and V_{BAT} monitoring

Table 92. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	26	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er(1)	Error on Q	–10	-	+10	%
t_{S_vbat}(1)	ADC sampling time when reading V_{BAT} input	9	-	-	µs
$V_{BAThigh}$	High supply monitoring	-	3.55	-	V
V_{BATlow}	Low supply monitoring	-	1.36	-	

1. Guaranteed by design.

Table 93. V_{BAT} charging characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS in PWR_CR3= 0	-	5	-	KΩ
		VBRS in PWR_CR3= 1		1.5	-	

Table 94. Temperature monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$TEMP_{high}$	High temperature monitoring	-	117	-	°C
$TEMP_{low}$	Low temperature monitoring	-	–25	-	

6.3.28 Voltage booster for analog switch

Table 95. Voltage booster for analog switch characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage	-	1.62	2.6	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	-	50	µs
$I_{DD(BOOST)}$	Booster consumption	$1.62\ V \leq V_{DD} \leq 2.7\ V$	-	-	125	µA
		$2.7\ V < V_{DD} < 3.6\ V$	-	-	250	

1. Guaranteed by characterization results.

6.3.29 Comparator characteristics

Table 96. COMP characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	3.3	3.6	V
V_{IN}	Comparator input voltage range	-	0	-	V_{DDA}	
V_{BG}	Scaler input voltage	-		(2)		
V_{SC}	Scaler offset voltage	-	-	±5	±10	mV
$I_{DDA(SCALER)}$	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)	-	0.2	0.3	µA
		BRG_EN=1 (bridge enable)	-	0.8	1	
t_{START_SCALER}	Scaler startup time	-	-	140	250	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	-	2	5	µs
		Medium mode	-	5	20	
		Ultra-low-power mode	-	15	80	
t_D(3)	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode	-	50	80	ns
		Medium mode	-	0.5	0.9	µs
		Ultra-low-power mode	-	2.5	7	
	Propagation delay for step > 200 mV with 100 mV overdrive only on positive inputs	High-speed mode	-	50	120	ns
		Medium mode	-	0.5	1.2	µs
		Ultra-low-power mode	-	2.5	7	
V_{offset}	Comparator offset error	Full common mode range	-	±5	±20	mV

Table 96. COMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		4	10	22	
		Medium hysteresis		8	20	37	
		High hysteresis		16	30	52	
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	800	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 17: Embedded reference voltage*.
3. Guaranteed by characterization results.

6.3.30 Operational amplifier characteristics

Table 97. Operational amplifier characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage Range	-	2	3.3	3.6	V
CMIR	Common Mode Input Range	-	0	-	V_{DDA}	
VI_{OFFSET}	Input offset voltage	25°C, no load on output	-	-	±1.5	mV
		All voltages and temperature, no load	-	-	±2.5	
ΔVI_{OFFSET}	Input offset voltage drift	-	-	±3.0	-	µV/°C
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage (0.1*V_{DDA})	-	-	1.1	1.5	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage (0.9*V_{DDA})	-	-	1.1	1.5	
I_{LOAD}	Drive current	-	-	-	500	µA
I_{LOAD_PGA}	Drive current in PGA mode	-	-	-	270	

Table 97. Operational amplifier characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{LOAD}	Capacitive load	-	-	-	50	pF
CMRR	Common mode rejection ratio	-	-	80	-	dB
PSRR	Power supply rejection ratio	C_{LOAD} ≤ 50pf / R_{LOAD} ≥ 4 kΩ(2) at 1 kHz, V_{com}=V_{DDA}/2	50	66	-	dB
GBW	Gain bandwidth for high supply range	200 mV ≤ Output dynamic range ≤ V_{DDA} - 200 mV	4	7.3	12.3	MHz
SR	Slew rate (from 10% and 90% of output voltage)	Normal mode	-	3	-	V/µs
		High-speed mode	-	24	-	
AO	Open loop gain	200 mV ≤ Output dynamic range ≤ V_{DDA} - 200 mV	59	90	129	dB
φm	Phase margin	-	-	55	-	°
GM	Gain margin	-	-	12	-	dB
V_{OHSAT}	High saturation voltage	I_{load}=max or R_{LOAD}=min, Input at V_{DDA}	V_{DDA} −100 mV	-	-	mV
V_{OLSAT}	Low saturation voltage	I_{load}=max or R_{LOAD}=min, Input at 0 V	-	-	100	
t_{WAKEUP}	Wake up time from OFF state	Normal mode: C_{LOAD} ≤ 50pf, R_{LOAD} ≥ 4 kΩ, follower configuration	-	0.8	3.2	µs
		High speed mode: C_{LOAD} ≤ 50pf, R_{LOAD} ≥ 4 kΩ, follower configuration	-	0.9	2.8	
PGA gain	Non inverting gain error value	PGA gain = 2	−1	-	1	%
		PGA gain = 4	−2	-	2	
		PGA gain = 8	−2.5	-	2.5	
		PGA gain = 16	−3	-	3	
	Inverting gain error value	PGA gain = 2	−1	-	1	
		PGA gain = 4	−1	-	1	
		PGA gain = 8	−2	-	2	
		PGA gain = 16	−3	-	3	
	External non-inverting gain error value	PGA gain = 2	−1	-	1	
		PGA gain = 4	−3	-	3	
		PGA gain = 8	−3.5	-	3.5	
		PGA gain = 16	−4	-	4	

Table 97. Operational amplifier characteristics[1] (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{network}$	R2/R1 internal resistance values in non-inverting PGA mode[3]	PGA Gain=2		-	10/10	-	kΩ/ kΩ
		PGA Gain=4		-	30/10	-	
		PGA Gain=8		-	70/10	-	
		PGA Gain=16		-	150/10	-	
	R2/R1 internal resistance values in inverting PGA mode[3]	PGA Gain = -1		-	10/10	-	
		PGA Gain = -3		-	30/10	-	
		PGA Gain = -7		-	70/10	-	
		PGA Gain = -15		-	150/10	-	
Delta R	Resistance variation (R1 or R2)	-		−15	-	15	%
PGA BW	PGA bandwidth for different non inverting gain	Gain=2		-	GBW/2	-	MHz
		Gain=4		-	GBW/4	-	
		Gain=8		-	GBW/8	-	
		Gain=16		-	GBW/16	-	
	PGA bandwidth for different inverting gain	Gain = -1		-	5.00	-	MHz
		Gain = -3		-	3.00	-	
		Gain = -7		-	1.50	-	
		Gain = -15		-	0.80	-	
en	Voltage noise density	at 1 KHz	output loaded with 4 kΩ	-	140	-	nV/√ Hz
		at 10 KHz		-	55	-	
$I_{DDA(OPAMP)}$	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode, follower	-	570	1000	µA
		High-speed mode		-	610	1200	

1. Guaranteed by design, unless otherwise specified.
2. R_{LOAD} is the resistive load connected to V_{SSA} or to V_{DDA}.
3. R2 is the internal resistance between the OPAMP output and th OPAMP inverting input. R1 is the internal resistance between the OPAMP inverting input and ground. PGA gain = 1 + R2/R1.

6.3.31 Digital filter for Sigma-Delta Modulators (DFSDM) characteristics

Unless otherwise specified, the parameters given in *Table 98* for DFSDM are derived from tests performed under the ambient temperature, fPCLKx frequency and supply voltage conditions summarized in *Table 12: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- VOS level set to VOS0

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (DìFSDM_CKINx, DFSDM_DATINx, DFSDM_CKOUT for DFSDM).

Table 98. DFSDM measured timing

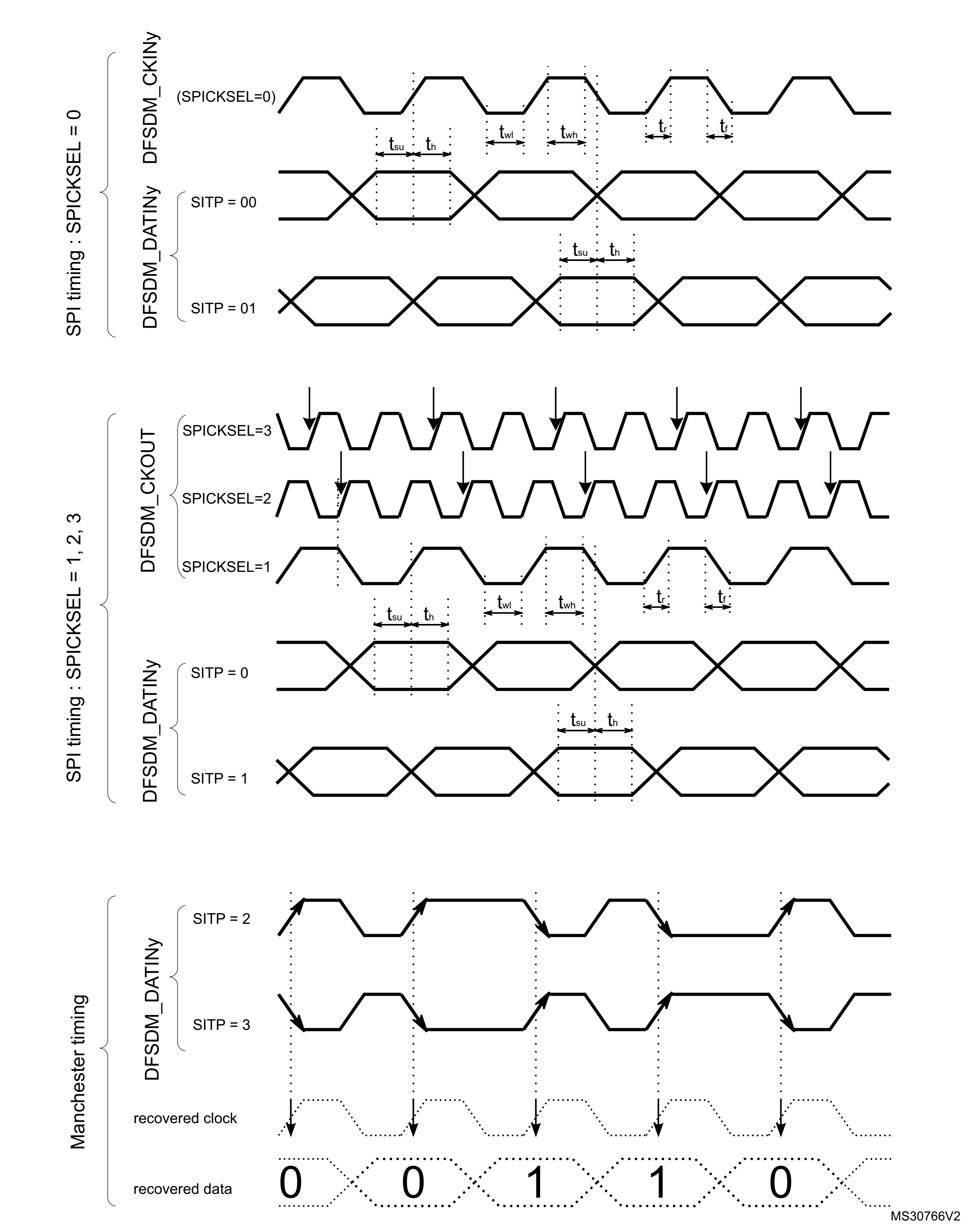
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	1.62 < V_{DD} < 3.6 V		-	-	(1)	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0] = 0,1), External clock mode (SPICKSEL[1:0] = 0)		-	-	20	MHz
		SPI mode (SITP[1:0] = 0,1), Internal clock mode (SPICKSEL[1:0] # 0)		-	-	20	MHz
f_{CKOUT}	Output clock frequency	1.62 < V_{DD} < 3.6 V		-	-	20	MHz
$DuCy_{CKOUT}$	Output clock frequency duty cycle	1.62 < V_{DD} < 3.6 V	Even division, CKOUTDIV = n, 1, 3, 5..	45	50	55	%
			Odd division, CKOUTDIV = n, 2, 4, 6..	(((n/2+1)/(n+1)) *100)−5	(((n/2+1)/(n+1)) *100)	(((n/2+1)/(n+1)) *100)+5	%

Table 98. DFSDM measured timing (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0] = 0,1), External clock mode (SPICKSEL[1:0] = 0)	$T_{CKIN}/2-0.5$	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0] = 0,1), External clock mode (SPICKSEL[1:0] = 0)	2	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0] = 0,1), External clock mode (SPICKSEL[1:0] = 0)	1	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0] = 2,3), Internal clock mode (SPICKSEL[1:0] # 0)	(CKOUTDIV+1) * $T_{DFSDMCLK}$	-	(2*CKOUTDIV) * $T_{DFSDMCLK}$	

1. The maximum DFSDM kernel clock frequency is specified in the RCC chapter of the reference manual (RM0468).

Figure 40. Channel transceiver timing diagrams



6.3.32 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 99* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage summarized in *Table 12: General operating conditions*, with the following configuration:

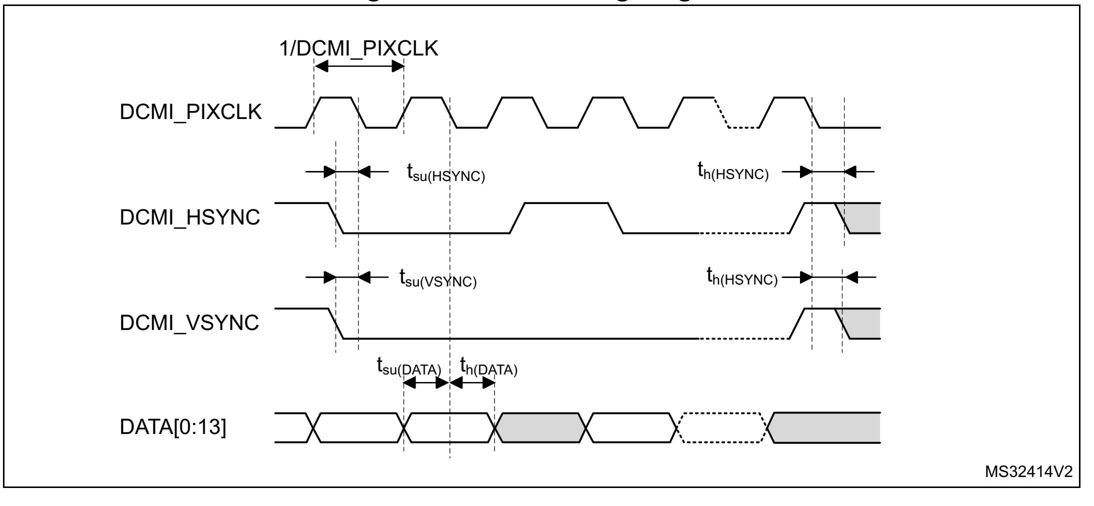
- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- VOS level set to VOS0

Table 99. DCMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	0.4	-
DCMI_PIXCLK	Pixel Clock input	-	110	MHz
D_{pixel}	Pixel Clock input duty cycle	30	70	%
t_{su}(DATA)	Data input setup time	2	-	ns
t_h(DATA)	Data hold time	1	-	ns
tsu(HSYNC), tsu(VSYNC)	DCMI_HSYNC/ DCMI_VSYNC input setup time	2	-	ns
th(HSYNC), th(VSYNC)	DCMI_HSYNC/ DCMI_VSYNC input hold time	1	-	ns

1. Guaranteed by characterization results.

Figure 41. DCMI timing diagram



6.3.33 Parallel synchronous slave interface (PSSI) characteristics

Unless otherwise specified, the parameters given in *Table 100* and *Table 101* for PSSI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage summarized in *Table 12: General operating conditions*.

Table 100. PSSI transmit characteristics(1)

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio PSSI_PDCK/f_{HCLK}	-	0.4	-
PSSI_PDCK	PSSI Clock input	-	50	MHz
		-	35(2)	
D_{pixel}	PSSI Clock input duty cycle	30	70	%
t_{ov}(DATA)	Data output valid time	-	10	ns
-	-	-	14(2)	
t_{oh}(DATA)	Data output hold time	4.5	-	
$t_{ov(}$(DE)	DE output valid time	-	10	
t_{oh}(DE)	DE output hold time	4	-	
tsu(RDY)	RDY input setup time	0	-	
th(RDY)	RDY input hold time	0	-	

1. Guaranteed by characterization results.
2. This value is obtained by using PA9, PA10 or PH4 I/O.

Table 101. PSSI receive characteristics(1)

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio PSSI_PDCK/f_{HCLK}	-	0.4	-
PSSI_PDCK	PSSI Clock input	-	110	MHz
D_{pixel}	PSSI Clock input duty cycle	30	70	%
t_{su}(DATA)	Data input setup time	1.5	-	ns
t_h(DATA)	Data input hold time	0.5	-	
$t_{su(}$(DE)	DE input setup time	2	-	
t_h(DE)	DE input hold time	1	-	
tov(RDY)	RDY output valid time	-	15	
toh(RDY)	RDY output hold time	5.5	-	

1. Guaranteed by characterization results.

6.3.34 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 102* for LCD-TFT are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage summarized in *Table 12: General operating conditions*, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: 0.5VDD
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS0

Table 102. LTDC characteristics(1)

Symbol	Parameter		Min	Max	Unit
f_{CLK}	LTDC clock output frequency	2.7<V_{DD}<3.6 V, 20 pF	-	150	MHz
		2.7<V_{DD}<3.6 V		133	
		1.62<V_{DD}<3.6 V		90/76.5(2)	
D_{CLK}	LTDC clock output duty cycle		45	55	%
$t_{w(CLKH)}$, $t_{w(CLKL)}$	Clock High time, low time		$t_{w(CLK)}$//2−0.5	$t_{w(CLK)}$/2+0.5	ns
$t_{v(DATA)}$	Data output valid time	2.7<V_{DD}<3.6 V	-	2.0	
		1.62<V_{DD}<3.6 V		2.5/6.5(2)	
$t_{h(DATA)}$	Data output hold time		0	-	
$t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$	HSYNC/VSYNC/DE output valid time	2.7<V_{DD}<3.6 V	-	1.5	
		1.62<V_{DD}<3.6 V	-	2.0	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$	HSYNC/VSYNC/DE output hold time		0	-	

1. Guaranteed by characterization results.
2. This value is valid when PA[9], PA[10], PA[11], PA[12], PA[15], PB[11], PH[4], PJ[8], PJ[9], PJ[10], PJ[11], PK[0], PK[1] or PK[2] is used.

Figure 42. LCD-TFT horizontal timing diagram

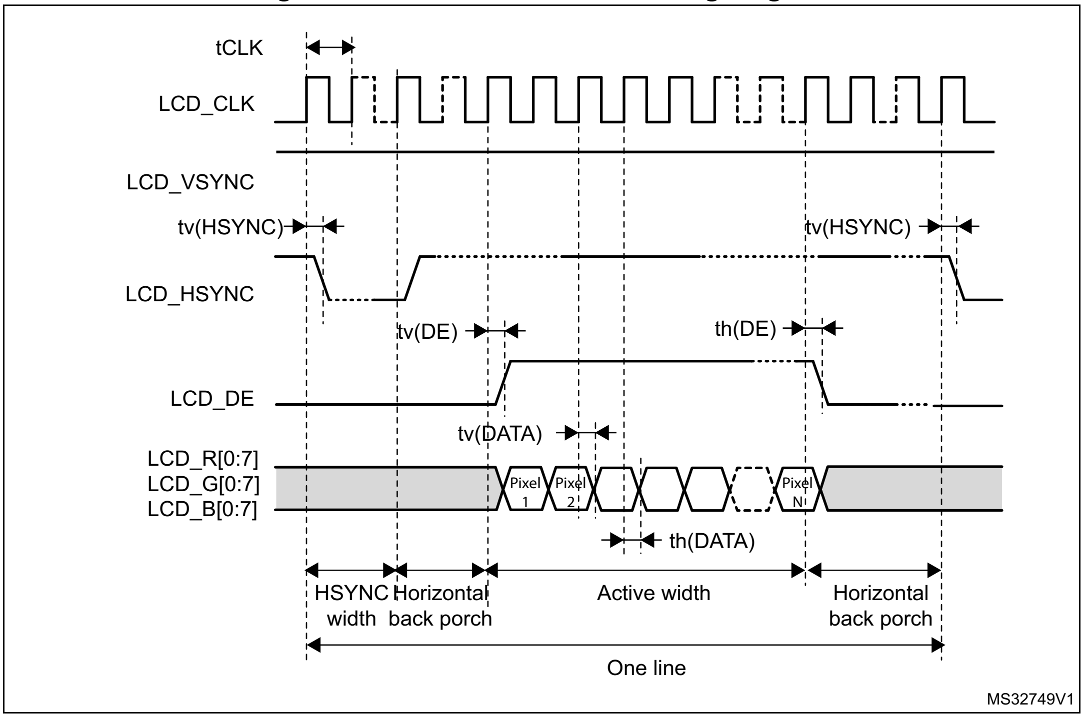
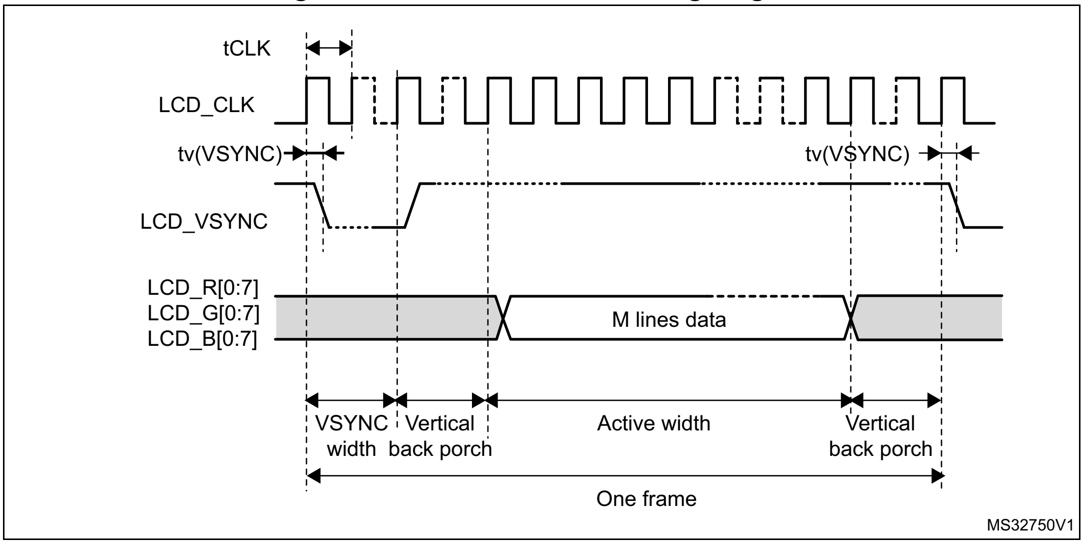


Figure 43. LCD-TFT vertical timing diagram



6.3.35 Timer characteristics

The parameters given in *Table 103* are guaranteed by design.

Refer to *Section 6.3.16: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 103. TIMx characteristics(1)(2)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 275 MHz	1	-	$t_{TIMxCLK}$
		AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 137.5 MHz	1	-	$t_{TIMxCLK}$
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 240 MHz	0	$f_{TIMxCLK}/2$	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$

1. TIMx is used as a general term to refer to the TIM1 to TIM17 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 or APB2 is up to 275 MHz, by setting the TIMPRE bit in the RCC_CFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = rcc_hclk1, otherwise TIMxCLK = 4x F_{rcc_pclkx1} or TIMxCLK = 4x F_{rcc_pclkx2}.

6.3.36 Low-power timer characteristics

The parameters given in *Table 104* are guaranteed by design.

Refer to *Section 6.3.16: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 104. LPTIMx characteristics(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	1	-	$t_{TIMxCLK}$
$f_{LPTIMxCLK}$	Timer kernel clock	0	137.5	MHz
f_{EXT}	Timer external clock frequency on Input1 and Input2	0	$f_{LPTIMxCLK}/2$	
Res_{TIM}	Timer resolution	-	16	bit
t_{MAX_COUNT}	Maximum possible count	-	65536	$t_{TIMxCLK}$

1. LPTIMx is used as a general term to refer to the LPTIM1 to LPTIM5 timers.
2. Guaranteed by design.

6.3.37 Communication interfaces

I^2C interface characteristics

The I^2C interface meets the timings requirements of the I^2C-bus specification and user manual revision 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I^2C timings requirements are guaranteed by design when the I^2C peripheral is properly configured (refer to RM0399 reference manual) and when the i2c_ker_ck frequency is greater than the minimum shown in the table below:

Table 105. Minimum i2c_ker_ck frequency in all I^2C modes

Symbol	Parameter	Condition		Min	Unit
f(I2CCLK)	I2CCLK frequency	Standard-mode	-	2	MHz
		Fast-mode	Analog Filtre ON DNF=0	8	
			Analog Filtre OFF DNF=1	9	
		Fast-mode Plus	Analog Filtre ON DNF=0	17	
			Analog Filtre OFF DNF=1	16	-

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but still present.
- The 20 mA output drive requirement in Fast-mode Plus is not supported. This limits the maximum load C_{Load} supported in Fm+, which is given by these formulas:

  $t_{r(SDA/SCL)}=0.8473xR_P * C_{Load}$

  $R_{P(min)}= (V_{DD}-V_{OL(max)})/I_{OL(max)}$

  Where R_P is the I2C lines pull-up. Refer to *Section 6.3.16: I/O port characteristics* for the I^2C I/Os characteristics.

All I^2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 106. I^2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by analog filter	50(2)	80(3)	ns

1. Guaranteed by characterization results.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered.

USART interface characteristics

Unless otherwise specified, the parameters given in Table 107 for USART are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 12: General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- VOS level set to VOS0

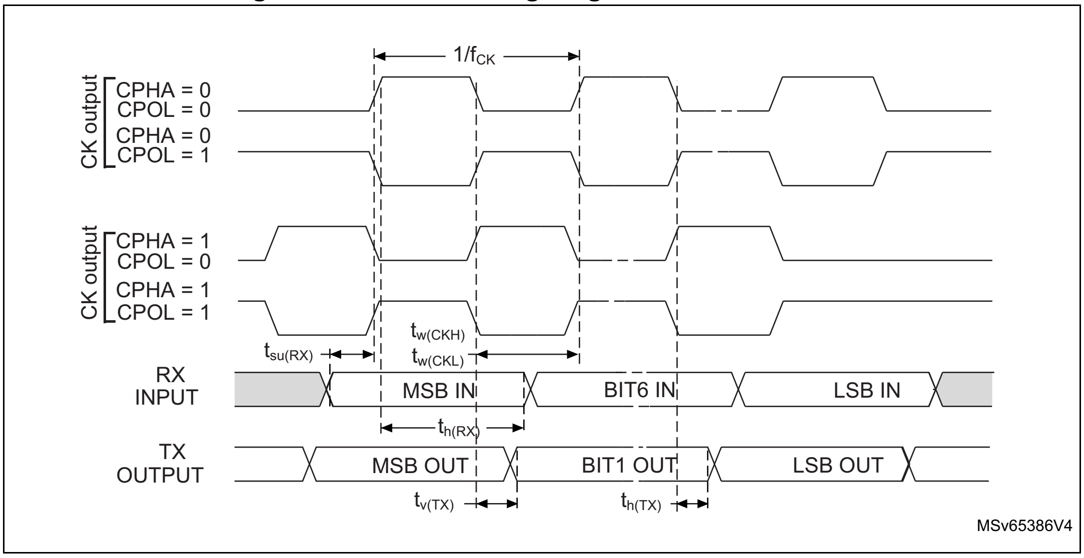
Refer to Section 6.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Table 107. USART characteristics[(1)]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master mode, 1.62 V < V_{DD} < 3.6 V	-	-	17.0	MHz
		Slave receiver mode, 1.62 V < V_{DD} < 3.6 V			45.0	
		Slave transmitter mode, 1.62 V < V_{DD} < 3.6 V	-	-	27.0	
		Slave transmitter mode, 2.5 V < V_{DD} < 3.6 V			37.0	
$t_{su(NSS)}$	NSS setup time	Slave mode	t_{ker}+1	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2	-	-	
$t_{w(CKH)}$, $t_{w(CKL)}$	CK high and low time	Master mode	$1/f_{CK}/2-2$	$1/f_{CK}/2$	$1/f_{CK}/2+2$	
$t_{su(RX)}$	Data input setup time	Master mode	16	-	-	
		Slave mode	1.0	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	0	-	-	
		Slave mode	2.0	-	-	
$t_{v(TX)}$	Data output valid time	Slave mode, , 1.62 V < V_{DD} < 3.6 V	-	12.0	18	
		Slave mode, , 2.5 V < V_{DD} < 3.6 V	-	12.0	13.5	
		Master mode	-	0.5	1	
$t_{h(TX)}$	Data output hold time	Slave mode	9	-	-	
		Master mode	0	-	-	

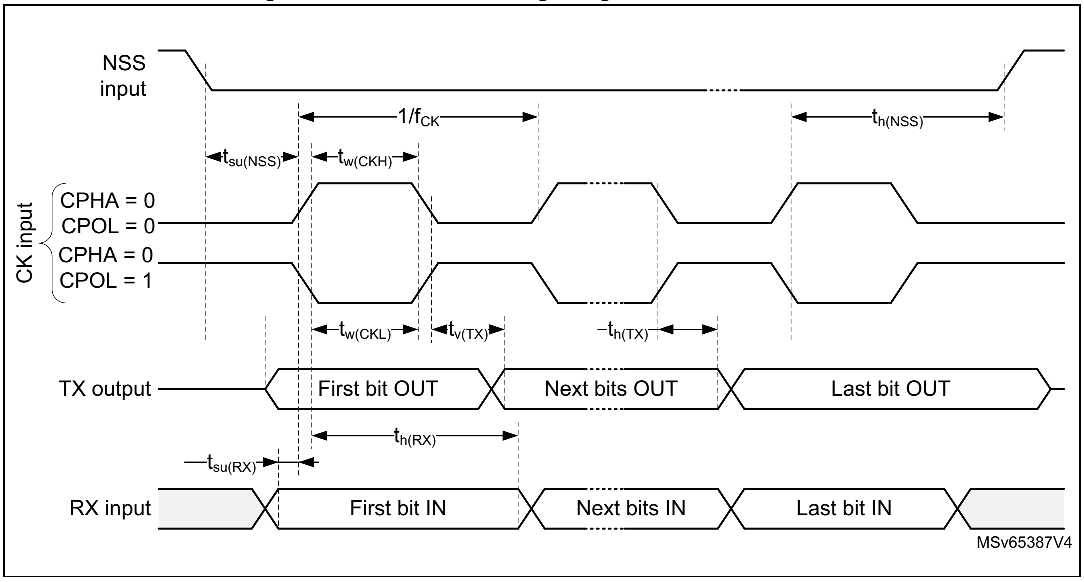
1. Guaranteed by characterization results.

Figure 44. USART timing diagram in master mode



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 45. USART timing diagram in slave mode



SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 108* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 12: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS0

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (SS, SCK, MOSI, MISO for SPI).

Table 108. SPI characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Master mode, 2.7 V < V_{DD} < 3.6 V, SPI1, 2, 3	-	-	125	MHz
		Master mode, 1.62 V < V_{DD} < 3.6 V, SPI1, 2, 3			80/66(3)	
		Master mode, 1.62 V < V_{DD} < 3.6 V, SPI4, 5, 6			68.5	
		Slave receiver mode, 1.62 V < V_{DD} < 3.6 V, SPI1, 2, 3			100	
		Slave receiver mode, 1.62 V < V_{DD} < 3.6 V, SPI4, 5, 6			68.5	
		Slave mode transmitter/full duplex, 2.7 V < V_{DD} < 3.6 V			45	
		Slave mode transmitter/full duplex, 1.62 V < V_{DD} < 3.6 V			42.5/31(4)	
$t_{su(NSS)}$	NSS setup time	Slave mode	2	-	-	-
$t_{h(NSS)}$	NSS hold time	Slave mode	1	-	-	
$t_{w(SCKH)}$, $t_{w(SCKL)}$	SCK high and low time	Master mode	$t_{SCK}/2-1$(5)	$t_{SCK}/2$(5)	$t_{SCK}/2+1$(5)	

Table 108. SPI characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(MI)}$	Data input setup time	Master mode	2.5	-	-	ns
$t_{su(SI)}$		Slave mode	1	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	3	-	-	
$t_{h(SI)}$		Slave mode	1.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	13	27	
$t_{dis(SO)}$	Data output disable time	Slave mode	0	1	5	
$t_{v(SO)}$	Data output valid time	Slave mode, 2.7 V < V_{DD} < 3.6 V	-	7.5	11	
		Slave mode, 1.62 V < V_{DD} < 3.6 V	-	7.5	12/16(4)	
$t_{v(MO)}$		Master mode, 1.62 V < V_{DD} < 3.6 V	-	1	1.5/5.5(6)	
$t_{h(SO)}$	Data output hold time	Slave mode	7	-	-	
$t_{h(MO)}$		Master mode	0.5	-	-	

1. Guaranteed by characterization results.
2. The values given in the above table might be degraded when PC3_C/PC2_C I/Os are used (not available on all packages).
3. This value is obtained by using PA9 or PA12 I/O.
4. This value is obtained by using PC2 or PJ11 I/O.
5. $t_{SCK} = t_{ker\_ck}$ * baud rate prescaler.
6. This value is obtained by using PC3 or PJ10 I/O.

Figure 46. SPI timing diagram - slave mode and CPHA = 0

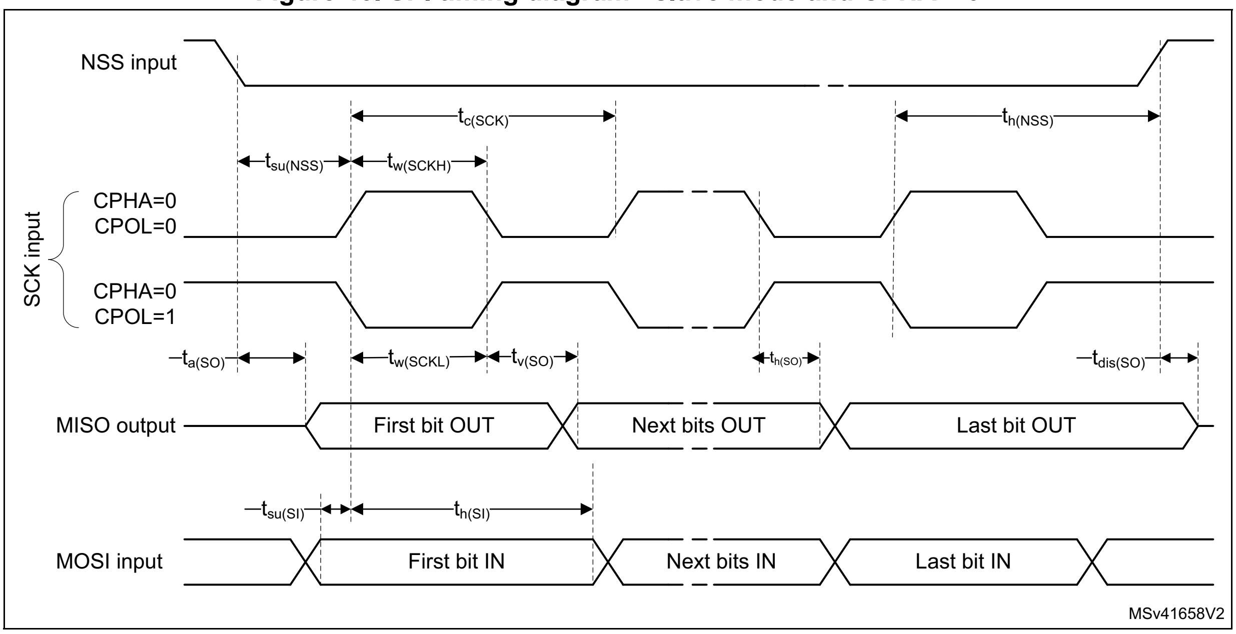


Figure 47. SPI timing diagram - slave mode and CPHA = 1

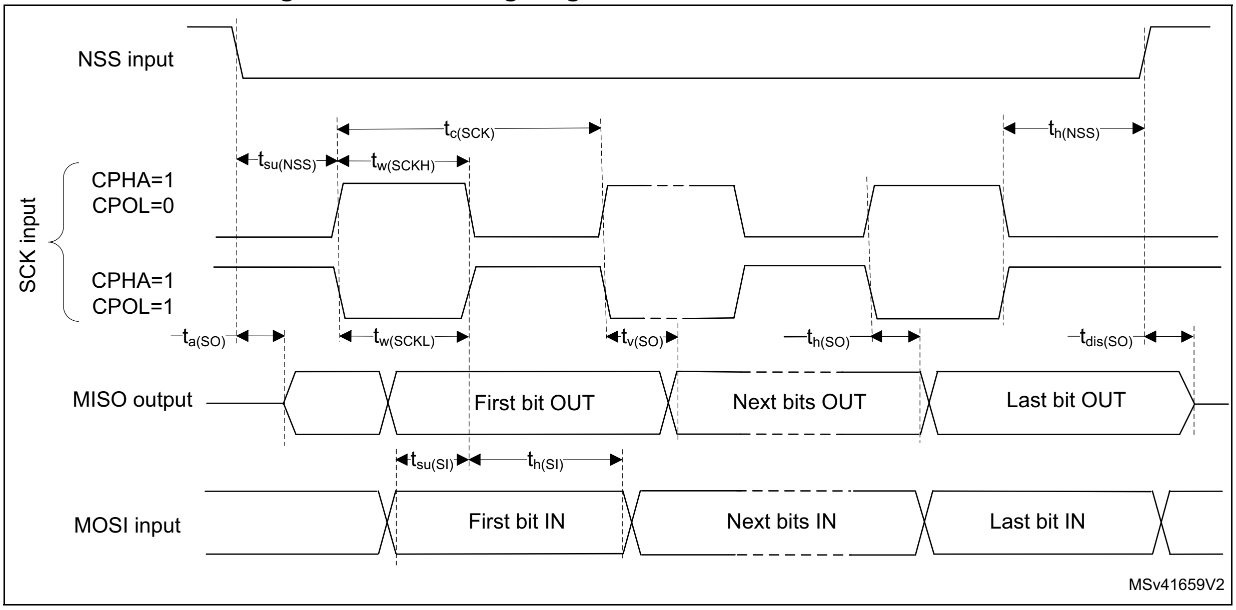
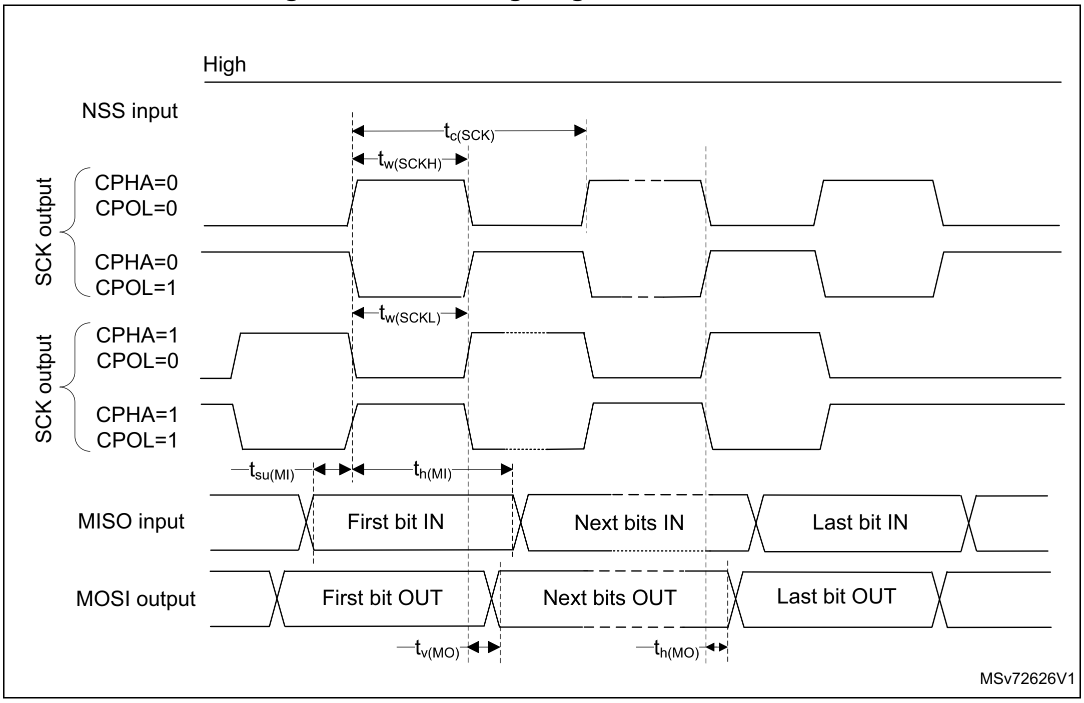


Figure 48. SPI timing diagram - master mode



I^2S Interface characteristics

Unless otherwise specified, the parameters given in *Table 109* for I^2S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 12: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS0

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,WS).

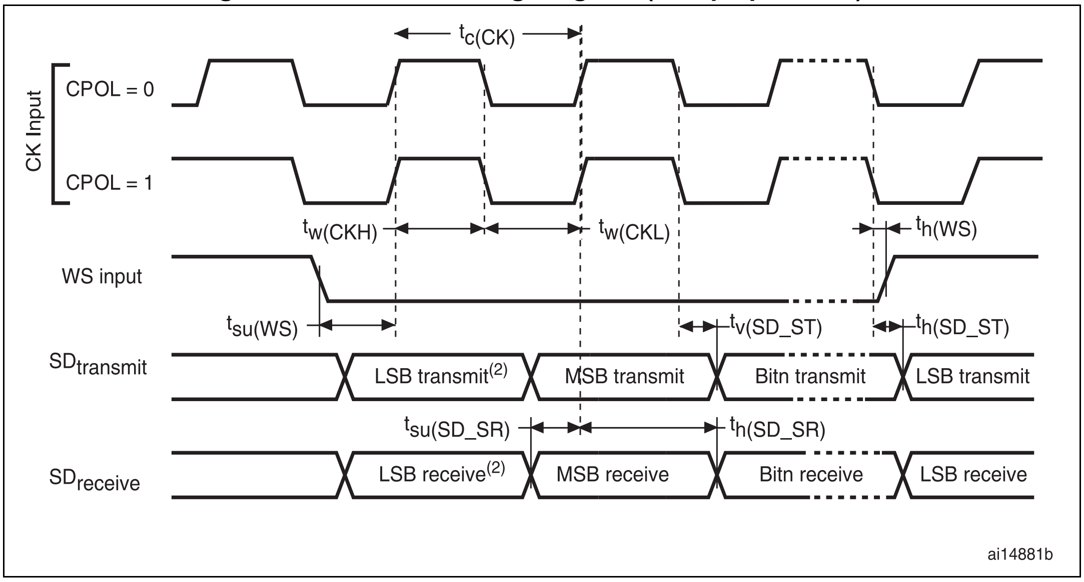
Table 109. I^2S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I^2S main clock output	-	-	50	MHz
		Master transmitter	-	50/40(2)	
		Master receiver	-	50/40(2)	
		Slave transmitter	-	41.5/31(3)	
		Slave receiver	-	50	
$t_{v(WS)}$	WS valid time	Master mode	-	2/6(4)	ns
$t_{h(WS)}$	WS hold time		1	-	
$t_{su(WS)}$	WS setup time	Slave mode	3	-	
$t_{h(WS)}$	WS hold time		1	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	2.5	-	
$t_{su(SD\_SR)}$		Slave receiver	1	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	3	-	
$t_{h(SD\_SR)}$		Slave receiver	1.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	12/16(3)	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	2/6(5)	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	6.5	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	0.5	-	

1. Guaranteed by characterization results.
2. This value is obtained when PA9 or PA12 are used.
3. This value is obtained when PC2 is used.
4. This value is obtained when PA11 or PA15 are used.

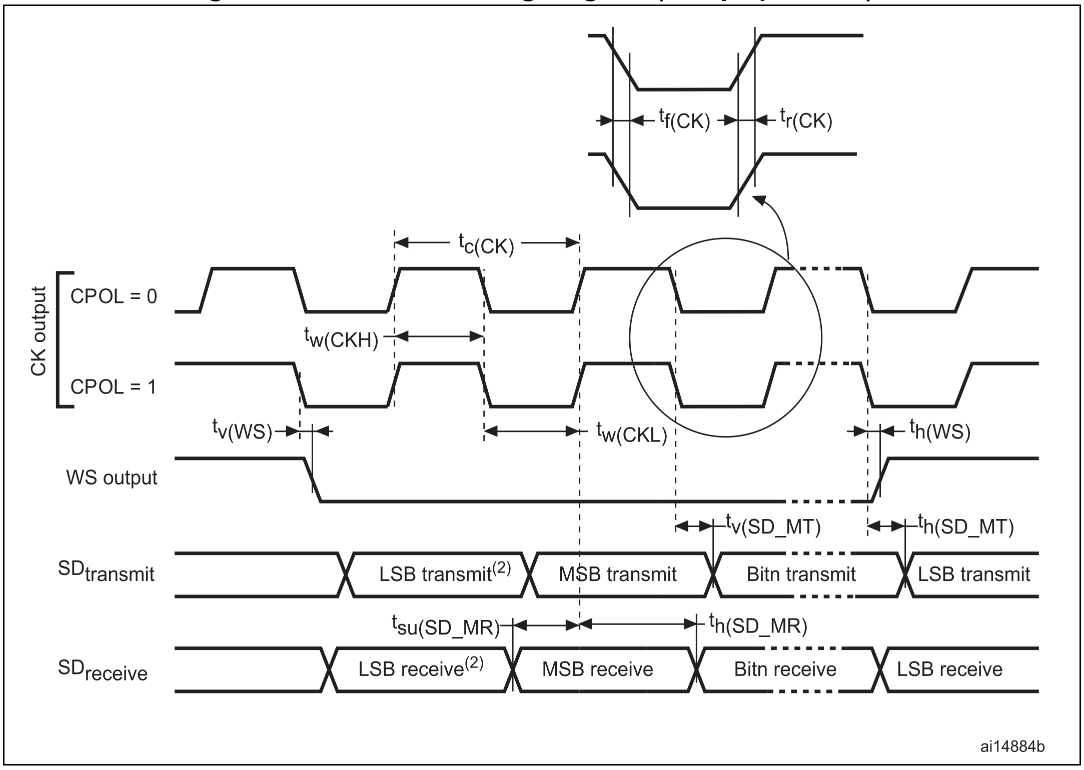
5. This value is obtained when PC3 is used.

Figure 49. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 50. I²S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

SAI characteristics

Unless otherwise specified, the parameters given in *Table 110* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in *Table 12: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- IO Compensation cell activated.
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- VOS level set to VOS0

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 110. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	SAI Main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency(2)	Master transmitter, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	45	MHz
		Master transmitter, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	32	
		Master receiver, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	32	
		Slave transmitter, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	47.5	
		Slave transmitter, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	41.5	
		Slave receiver, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	50	

Table 110. SAI characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(FS)}$	F_S valid time	Master mode, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	11	ns
		Master mode, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	15.5	
$t_{su(FS)}$	F_S setup time	Slave mode	2.5	-	
$t_{h(FS)}$	F_S hold time	Master mode	6	-	
		Slave mode	0.5	-	
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	3	-	
$t_{su(SD\_B\_SR)}$		Slave receiver	3.5	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	3.5	-	
$t_{h(SD\_B\_SR)}$		Slave receiver	0	-	
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge), 2.7 V ≤ V_{DD} ≤ 3.6 V	-	10.5	
		Slave transmitter (after enable edge), 1.62 V ≤ V_{DD} ≤ 3.6 V	-	12	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	6.5	-	
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge), 2.7 V ≤ V_{DD} ≤ 3.6 V	-	10.5	
		Master transmitter (after enable edge), 1.62 V ≤ V_{DD} ≤ 3.6 V	-	14.5	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	6	-	

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.

Figure 51. SAI master timing waveforms

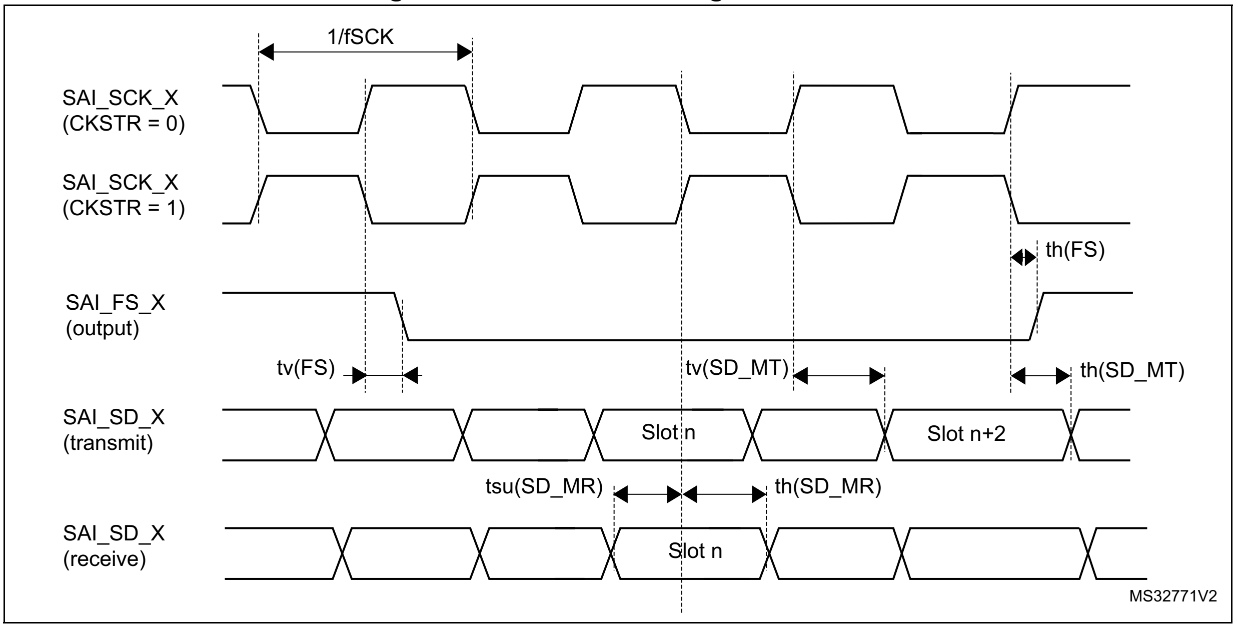
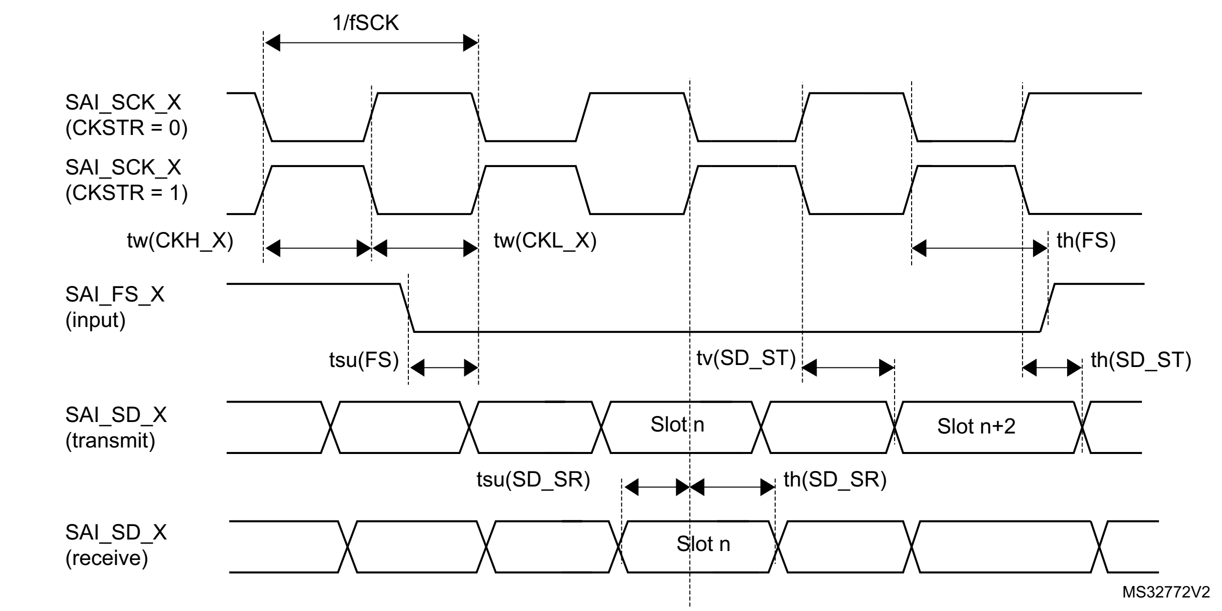


Figure 52. SAI slave timing waveforms



MDIO characteristics

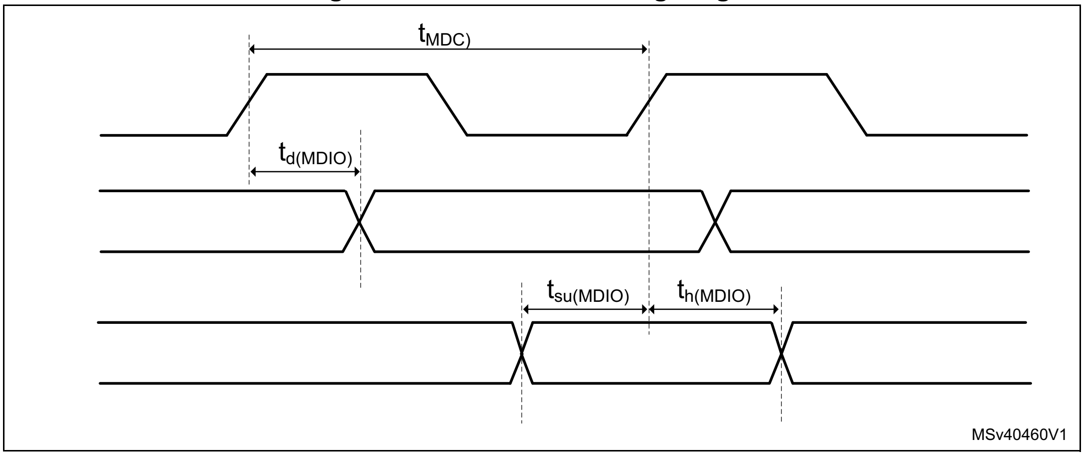
Unless otherwise specified, the parameters given in *Table 111* for the MDIO are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in *Table 12: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- I/O Compensation cell activated.
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS0

Table 111. MDIO slave timing parameters

Symbol	Parameter	Min	Typ	Max	Unit
F_{MDC}	Management Data Clock	-	-	30	MHz
$t_{d(MDIO)}$	Management Data Iput/output output valid time	8	10	18	ns
$t_{su(MDIO)}$	Management Data Iput/output setup time	1	-	-	
$t_{h(MDIO)}$	Management Data Iput/output hold time	1	-	-	

Figure 53. MDIO slave timing diagram



SD/SDIO MMC card host interface (SDMMC) characteristics

Unless otherwise specified, the parameters given in *Table 112* and *Table 113* for SDIO are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage summarized in *Table 12: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS0

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output characteristics.

Table 112. Dynamics characteristics: SD / MMC characteristics, V_{DD} = 2.7 to 3.6 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	120	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} =52MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR/DDR mode						
t_{ISU}	Input setup time HS	-	2.5	-	-	ns
t_{IH}	Input hold time HS	-	0.5	-	-	
t_{IDW}(3)	Input valid window (variable window)	-	1.5	-	-	
CMD, D outputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR/DDR mode						
t_{OV}	Output valid time HS	-	-	5.5	6	ns
t_{OH}	Output hold time HS	-	4.5	-	-	

Table 112. Dynamics characteristics: SD / MMC characteristics, V_{DD} = 2.7 to 3.6 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	-	1.5		-	ns
t_{IHD}	Input hold time SD	-	0.5		-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	-	-	1	1	ns
t_{OHD}	Output hold default time SD	-	0	-	-	

1. Guaranteed by characterization results.
2. Above 100 MHz, C_L = 20 pF.
3. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Table 113. Dynamics characteristics: eMMC characteristics VDD = 1.71V to 1.9V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	85	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} =52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	-	1.5	-	-	ns
t_{IH}	Input hold time HS	-	1.5	-	-	
t_{IDW}(3)	Input valid window (variable window)	-	3.5	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OVD}	Output valid time HS	-	-	6	6.5	ns
t_{OHD}	Output hold time HS	-	5.5	-	-	

1. Guaranteed by characterization results.
2. C_L = 20 pF.
3. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Figure 54. SD high-speed mode

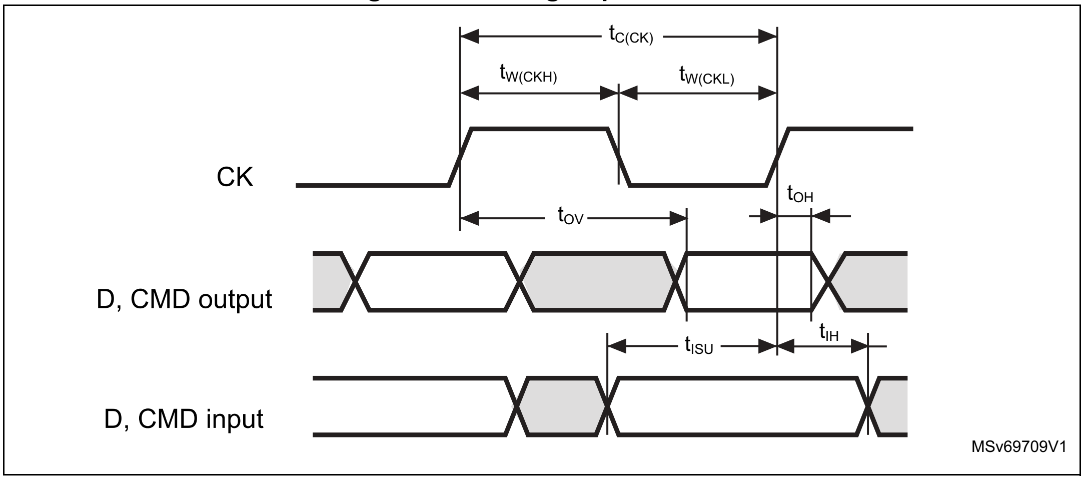


Figure 55. SD default mode

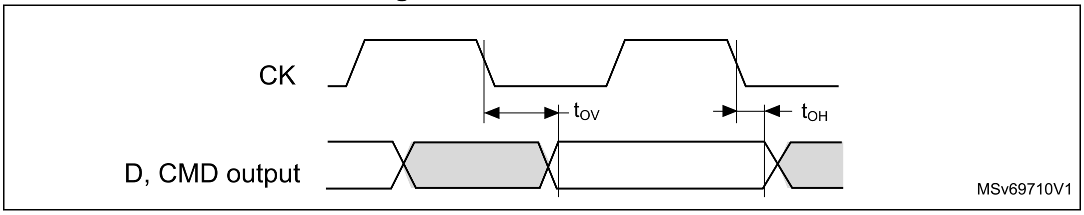
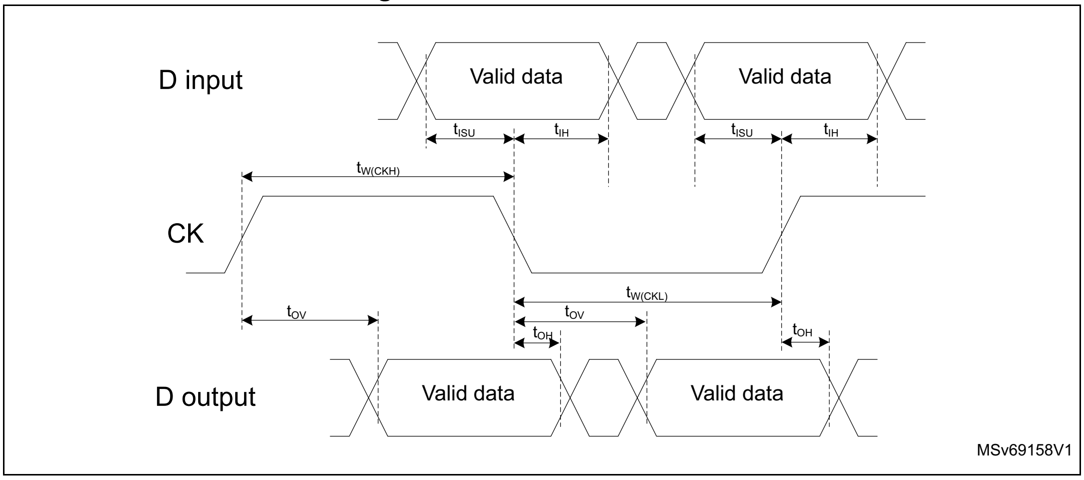


Figure 56. SDMMC DDR mode



USB OTG_FS characteristics

Unless otherwise specified, the parameters given in *Table 115* for ULPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage summarized in *Table 12: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L=20 pF
- Measurement points are done at CMOS levels: 0.5V_{DD}
- IO Compensation cell activated.
- VOS level set to VOS0

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output characteristics.

Table 114. USB OTG_FS electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{DD33USB}$	USB transceiver operating voltage	-	3.0[1]	-	3.6	V
R_{PUI}	Embedded USB_DP pull-up value during idle	-	900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception	-	1400	2300	3200	
Z_{DRV}	Output driver impedance[2]	Driver high and low	28	36	44	

1. The USB functionality is ensured down to 2.7 V. However, not all USB electrical characteristics are degraded in the 2.7 to 3.0 V voltage range.
2. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

USB OTG_HS characteristics

Unless otherwise specified, the parameters given in *Table 115* for ULPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage summarized in *Table 12: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L=20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- VOS level set to VOS0

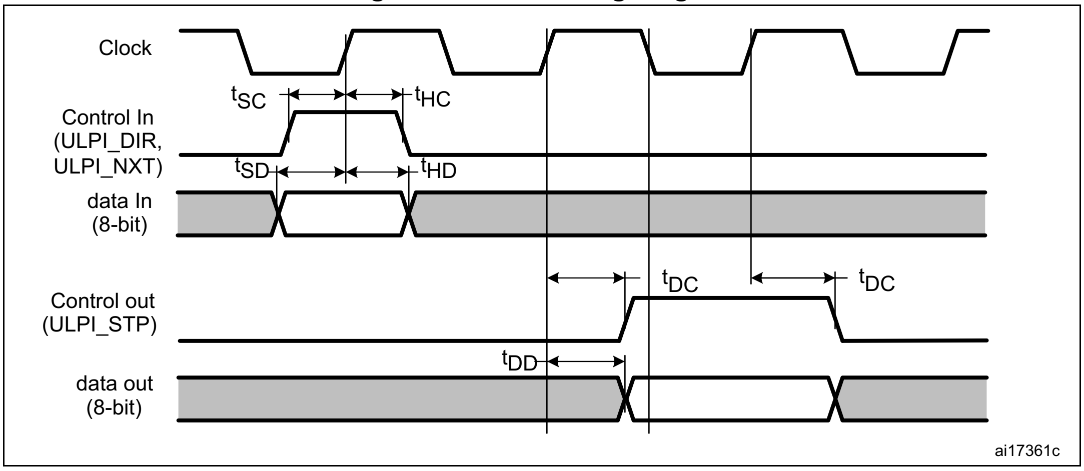
Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output characteristics.

Table 115. Dynamics characteristics: USB ULPI[1]

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{SC}	Control in (ULPI_DIR , ULPI_NXT) setup time	-	5.5	-	-	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	-	0	-	-	
t_{SD}	Data in setup time	-	2.5	-	-	
t_{HD}	Data in hold time	-	0	-	-	
t_{DC}/t_{DD}	Control/Datal output delay	2.7 V < V_{DD} < 3.6 V, C_L = 20 pF	-	6.0	8.0	
		1.71 V < V_{DD} < 3.6 V , C_L = 15 pF	-	6.0	12	

1. Guaranteed by characterization results.

Figure 57. ULPI timing diagram



Ethernet interface characteristics

Unless otherwise specified, the parameters given in *Table 116*, *Table 117* and *Table 118* for SMI, RMII and MII are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and V_{DD} supply voltage conditions summarized in *Table 12: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L=20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS1

Due to timing constraint Pxy_C I/Os cannot be used as ethernet signals.

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output characteristics:

Table 116. Dynamics characteristics: Ethernet MAC signals for SMI (1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.5 MHz)	400	400	403	ns
$T_{d(MDIO)}$	Write data valid time	0.5	1.5	4	
$t_{su(MDIO)}$	Read data setup time	12.5	-	-	
$t_{h(MDIO)}$	Read data hold time	0	-	-	

1. Guaranteed by characterization results.

Figure 58. Ethernet SMI timing diagram

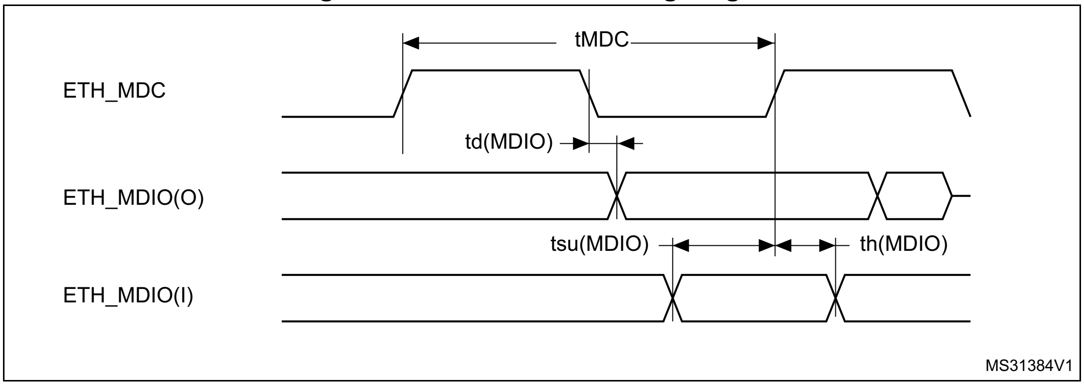


Table 117. Dynamics characteristics: Ethernet MAC signals for RMII (1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2	-	-	
$t_{su(CRS)}$	Carrier sense setup time	1.5	-	-	
$t_{ih(CRS)}$	Carrier sense hold time	1.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	8	9	10.5	
$t_{d(TXD)}$	Transmit data valid delay time	7	8	9.5	

1. Guaranteed by characterization results.

Figure 59. Ethernet RMII timing diagram

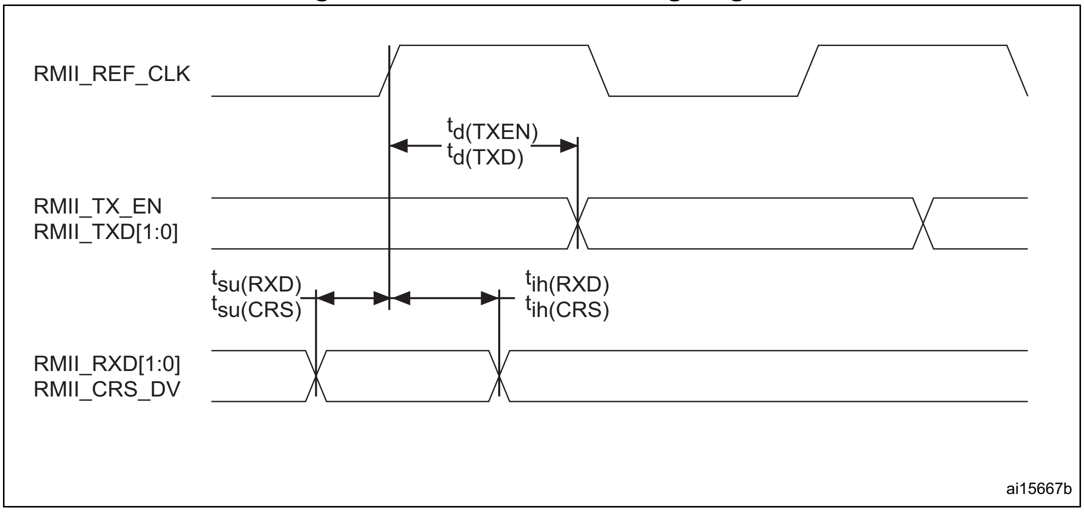
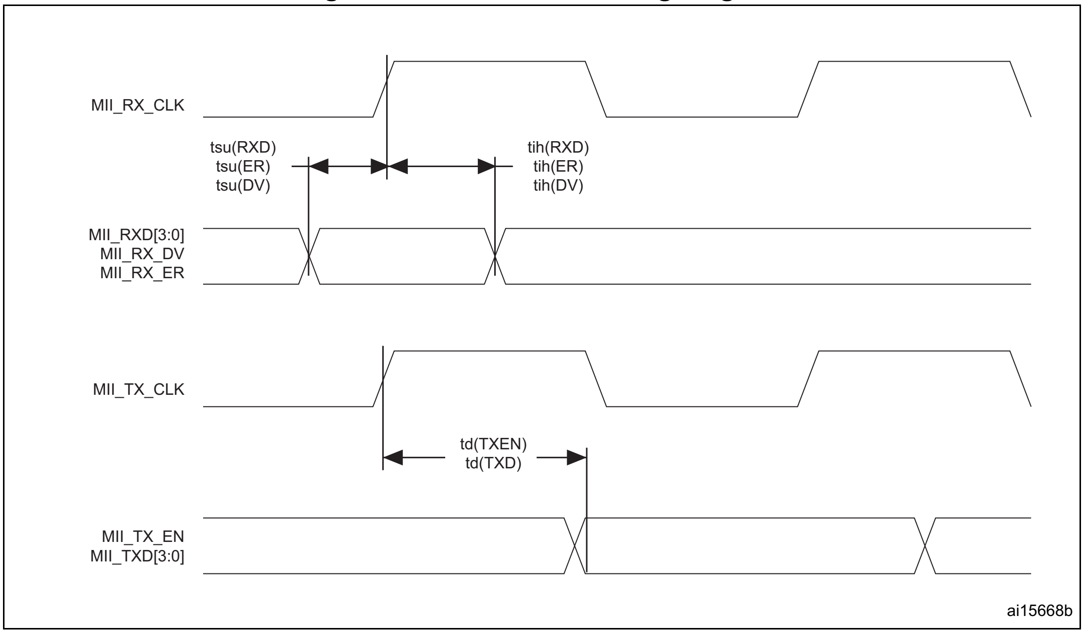


Table 118. Dynamics characteristics: Ethernet MAC signals for MII (1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2.0	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2.0	-	-	
$t_{su(DV)}$	Data valid setup time	1.5	-	-	
$t_{ih(DV)}$	Data valid hold time	1.5	-	-	
$t_{su(ER)}$	Error setup time	1.5	-	-	
$t_{ih(ER)}$	Error hold time	0.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	9.0	11	19	
$t_{d(TXD)}$	Transmit data valid delay time	8.5	10	19	

1. Guaranteed by characterization results.

Figure 60. Ethernet MII timing diagram



JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in *Table 119* and *Table 120* for JTAG/SWD are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and V_{DD} supply voltage summarized in *Table 12: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- VOS level set to VOS0

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output characteristics:

Table 119. Dynamics JTAG characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	T_{CK} clock frequency	2.7V <V_{DD}< 3.6 V	-	-	37	MHz
$1/t_{c(TCK)}$		1.62 <V_{DD}< 3.6 V	-	-	27.5	
$ti_{su(TMS)}$	TMS input setup time	-	2.5	-	-	
$ti_{h(TMS)}$	TMS input hold time	-	1	-	-	
$ti_{su(TDI)}$	TDI input setup time	-	1.5	-	-	-
$ti_{h(TDI)}$	TDI input hold time	-	1	-	-	-
$t_{ov(TDO)}$	TDO output valid time	2.7V <V_{DD}< 3.6 V	-	8	13.5	-
		1.62 <V_{DD}< 3.6 V	-	8	18	-
$t_{oh(TDO)}$	TDO output hold time	-	7	-	-	-

Table 120. Dynamics SWD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	SWCLK clock frequency	2.7V <V_{DD}< 3.6 V	-	-	71	MHz
$1/t_{c(SWCLK)}$		1.62 <V_{DD}< 3.6 V	-	-	52.5	
$ti_{su(SWDIO)}$	SWDIO input setup time	-	2.5	-	-	-
$ti_{h(SWDIO)}$	SWDIO input hold time	-	1	-	-	-
$t_{ov(SWDIO)}$	SWDIO output valid time	2.7V <V_{DD}< 3.6 V	-	8.5	14	-
		1.62 <V_{DD}< 3.6 V	-	8.5	19	-
$t_{oh(SWDIO)}$	SWDIO output hold time	-	8	-	-	-

Figure 61. JTAG timing diagram

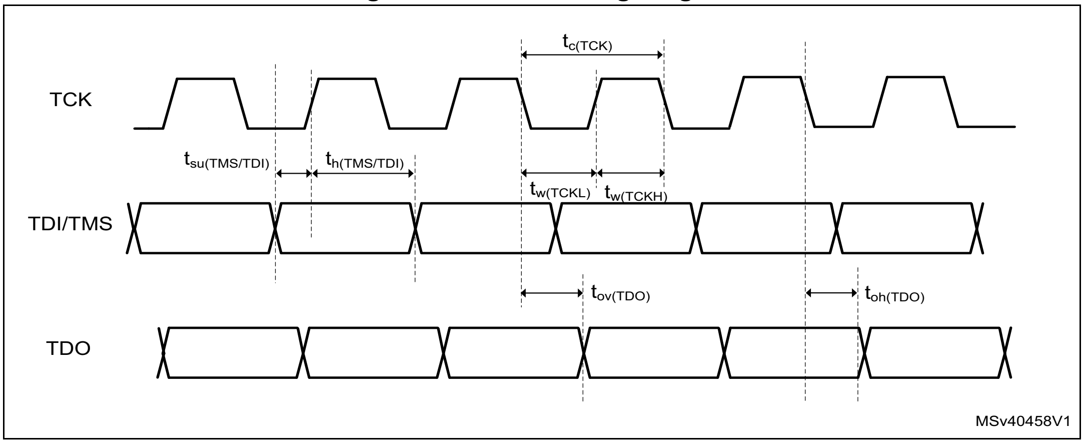
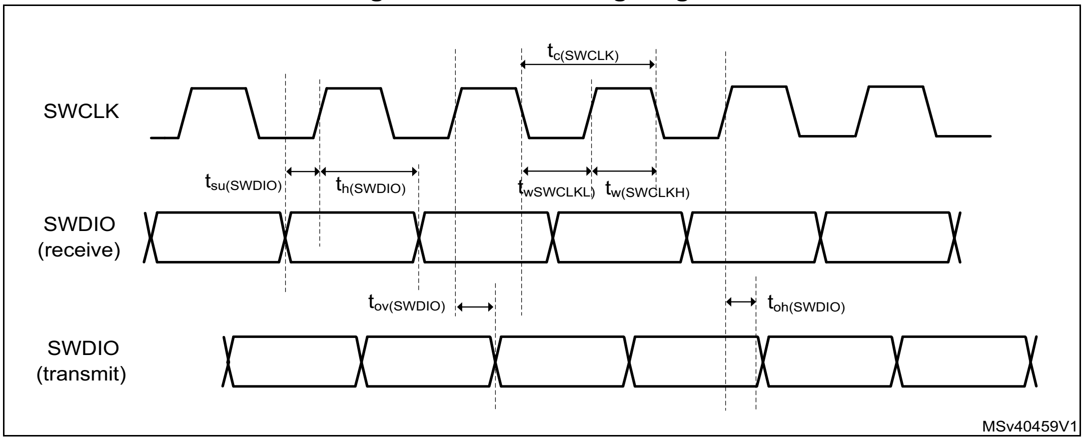


Figure 62. SWD timing diagram



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status *are available at www.st.com.* ECOPACK is an ST trademark.

7.1 Device marking

Refer to technical note "Reference device marking schematics for STM32 microcontrollers and microprocessors" (TN1433) available on *www.st.com*, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as "ES", "E" or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

7.2 LQFP100 package information (1L)

This LQFP is 100 lead, 14 x 14 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 63. LQFP100 - Outline(15)

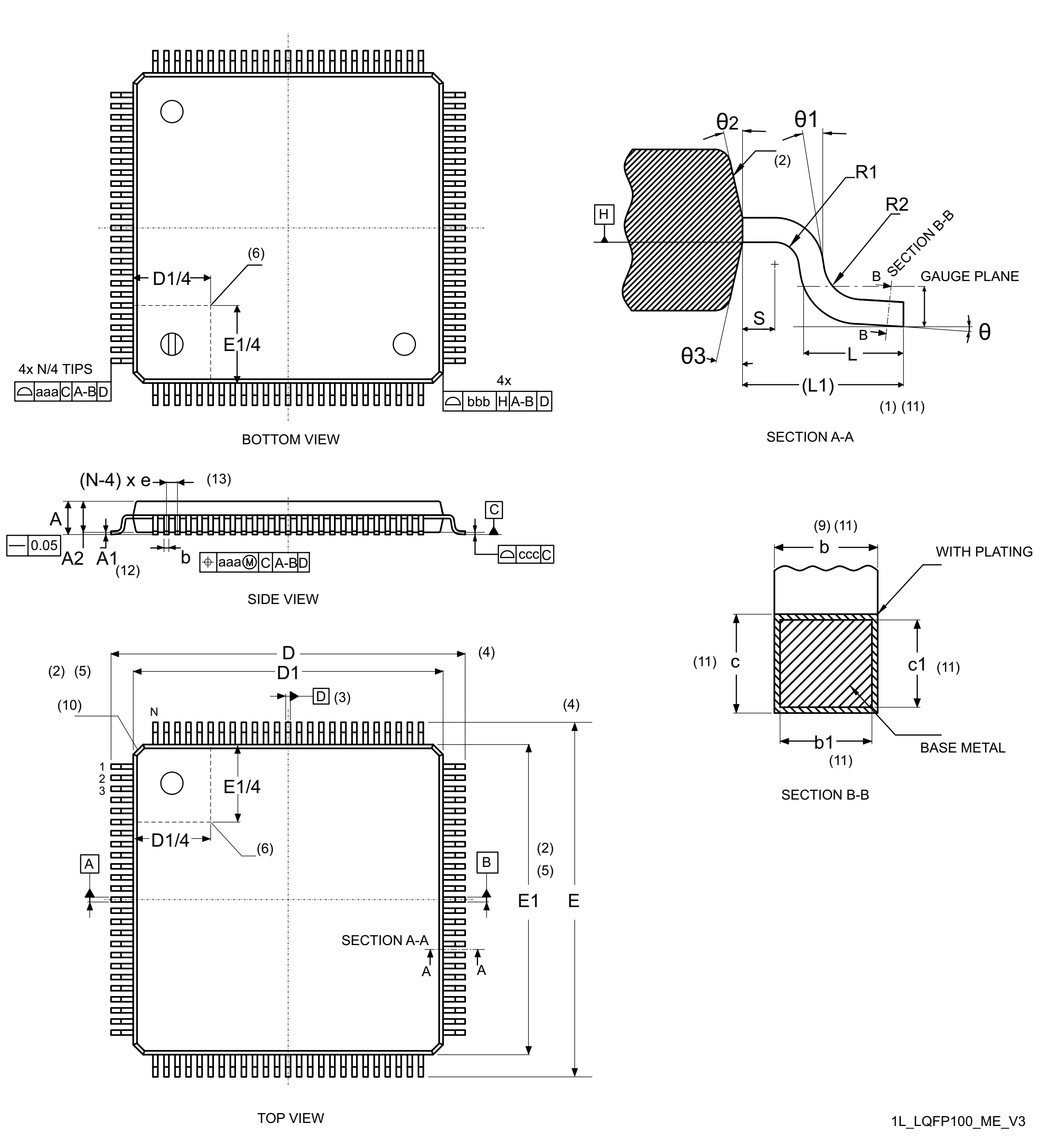


Table 121. LQFP100 - Mechanical data

Symbol	millimeters			inches(14)		
	Min	Typ	Max	Min	Typ	Max
A	-	1.50	1.60	-	0.0590	0.0630
A1(12)	0.05	-	0.15	0.0019	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0570

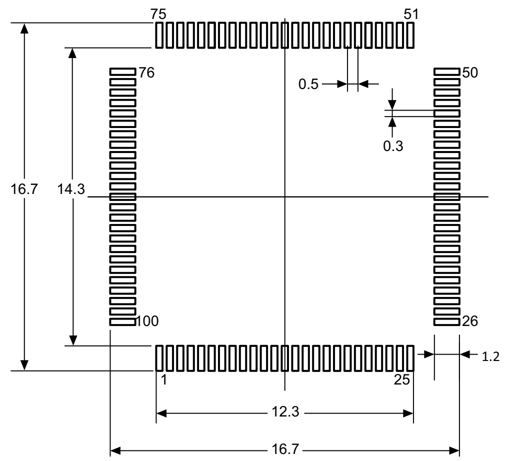
Table 121. LQFP100 - Mechanical data (continued)

Symbol	millimeters			inches(14)		
	Min	Typ	Max	Min	Typ	Max
b(9)(11)	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1(11)	0.17	0.20	0.23	0.0067	0.0079	0.0090
c(11)	0.09	-	0.20	0.0035	-	0.0079
c1(11)	0.09	-	0.16	0.0035	-	0.0063
D(4)	16.00 BSC			0.6299 BSC		
D1(2)(5)	14.00 BSC			0.5512 BSC		
E(4)	16.00 BSC			0.6299 BSC		
E1(2)(5)	14.00 BSC			0.5512 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.177	0.0236	0.0295
L1(1)(11)	1.00			-	0.0394	-
N(13)	100					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa(1)	0.20			0.0079		
bbb(1)	0.20			0.0079		
ccc(1)	0.08			0.0031		
ddd(1)	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 64. LQFP100 - Footprint example



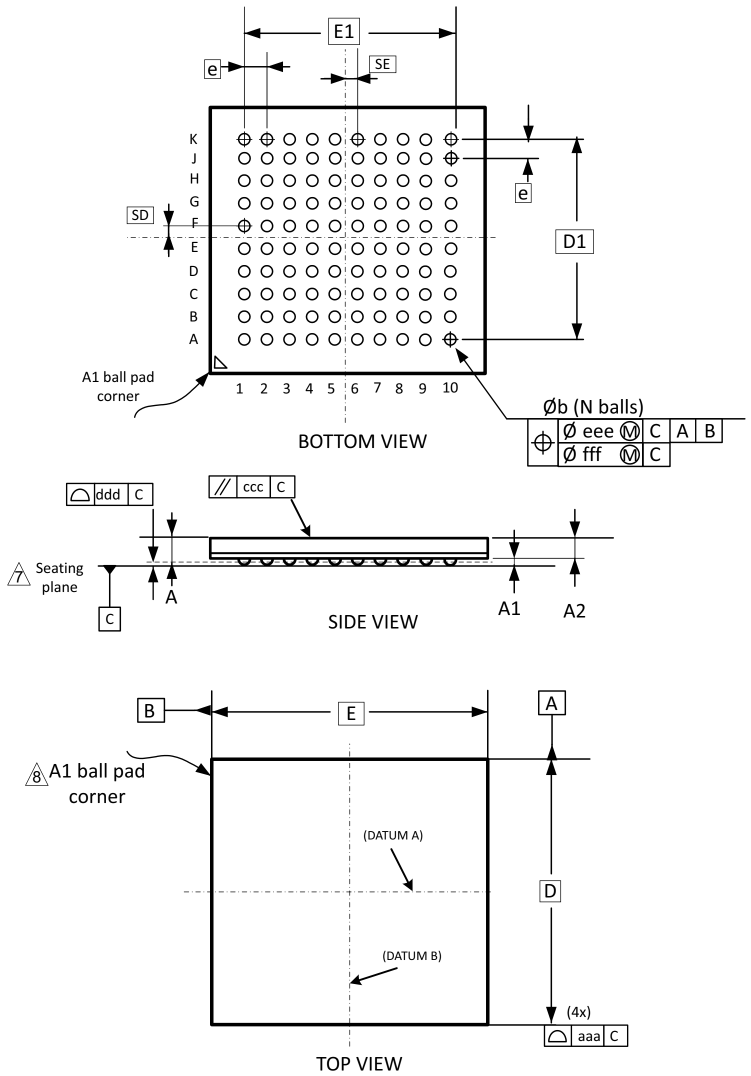
1. Dimensions are expressed in millimeters.

7.3 TFBGA100 package information (A08Q)

This TFBGA is 100 - ball, 8X8 mm, 0.8 mm pitch fine pitch ball grid array package.

Note: See list of notes in the notes section.

Figure 65. TFBGA100 - Outline(13)



A08Q_UFBGA100_ME_V2

Table 122. TFBGA100 - Mechanical data

Symbol	millimeters[1]			inches[12]		
	Min	Typ	Max	Min	Typ	Max
A[2][3]	-	-	1.20	-	-	0.0472
A1[4]	0.15	-	-	0.0059	-	-
A2	-	0.74	-	-	0.0291	-
b[5]	0.35	0.40	0.45	0.0138	0.0157	0.0177
D	8.00 BSC[6]			0.3150 BSC		
D1	7.20 BSC			0.2835 BSC		
E	8.00 BSC			0.3150 BSC		
E1	7.20 BSC			0.2835 BSC		
e[9]	0.80 BSC			0.0315 BSC		
N[11]	100					
SD[12]	0.40 BSC			0.0157 BSC		
SE[12]	0.40 BSC			0.0157 BSC		
aaa	0.15			0.0059		
ccc	0.20			0.0079		
ddd	0.10			0.0039		
eee	0.15			0.0059		
fff	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2018.
2. TFBGA stands for thin profile fine pitch ball grid array: 1.00 mm < A ≤ 1.20 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metalized markings, or other feature of package body or

integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to 4 decimal digits.
13. Drawing is not to scale.

Figure 66. TFBGA100 - Footprint example

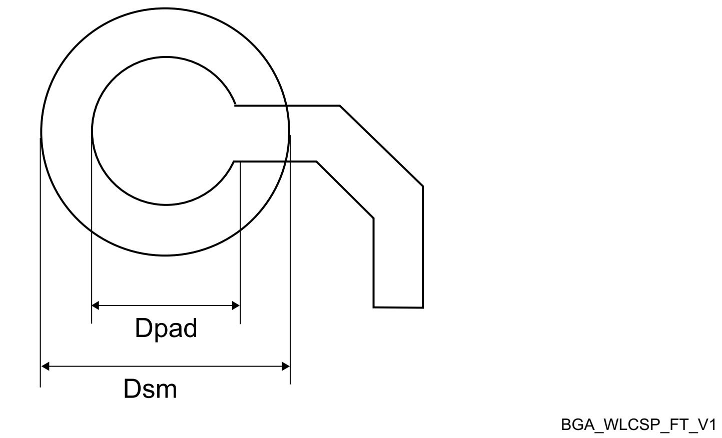


Table 123. TFBGA100 - Example of PCB design rules (0.8 mm pitch BGA)

Dimension	Values
Pitch	0.8
Dpad	0.400 mm
Dsm	0.470 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

7.4 LQFP144 package information (1A)

This LQFP is a 144-pin, 20 x 20 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 67. LQFP144 - Outline(15)

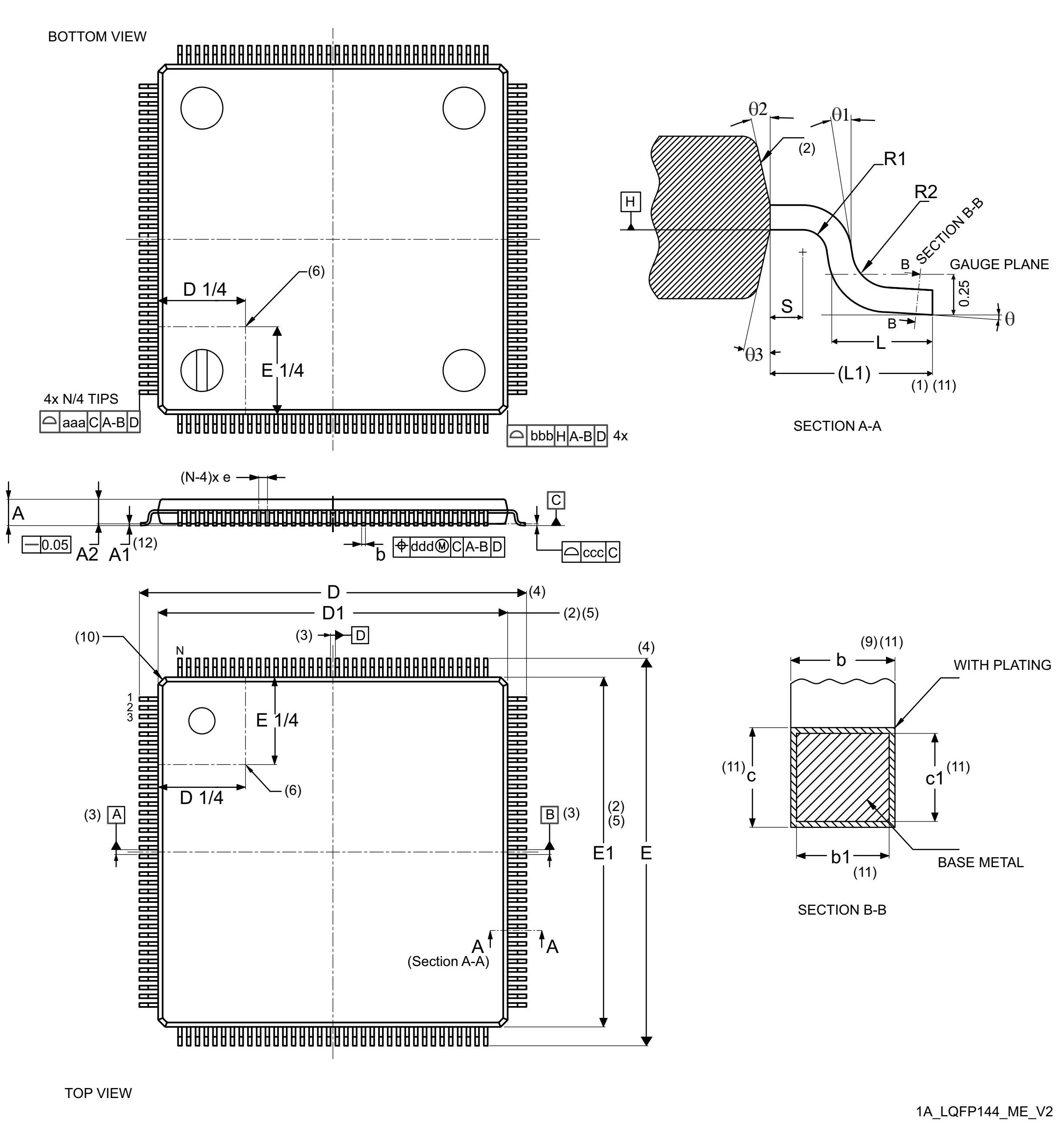


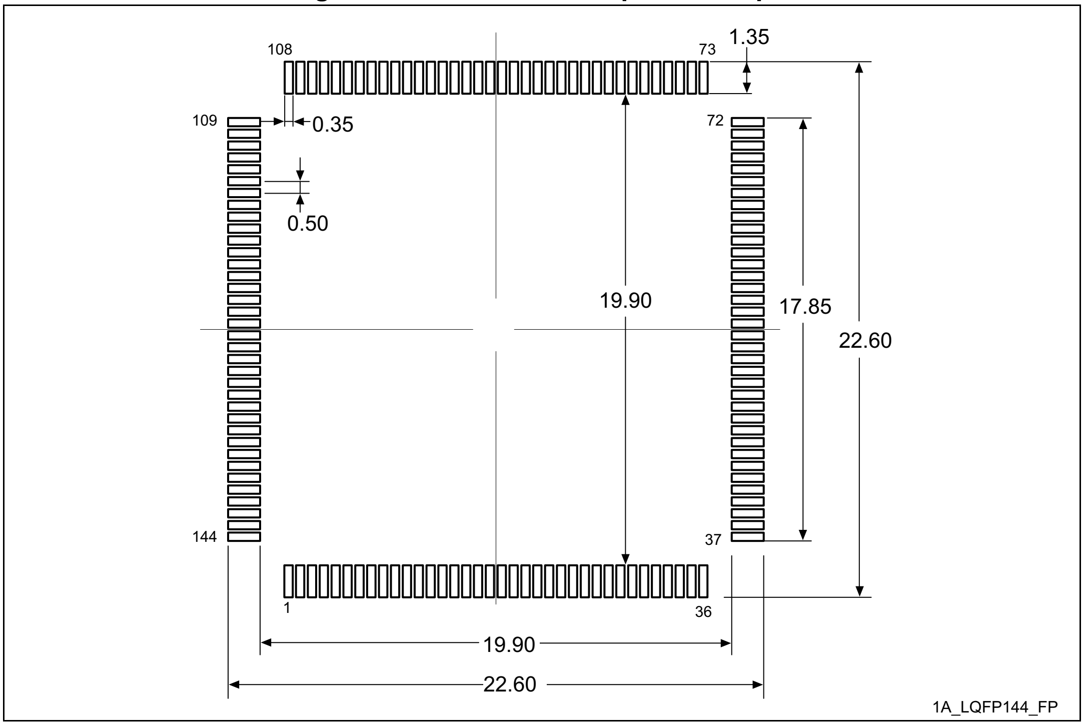
Table 124. LQFP144 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	22.00 BSC			0.8661 BSC		
D1[2][5]	20.00 BSC			0.7874 BSC		
E[4]	22.00 BSC			0.8661 BSC		
E1[2][5]	20.00 BSC			0.7874 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	144					
θ	0°	3.5°	7°	0°	3.5°	7°
$\theta 1$	0°	-	-	0°	-	-
$\theta 2$	10°	12°	14°	10°	12°	14°
$\theta 3$	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa	0.20			0.0079		
bbb	0.20			0.0079		
ccc	0.08			0.0031		
ddd	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

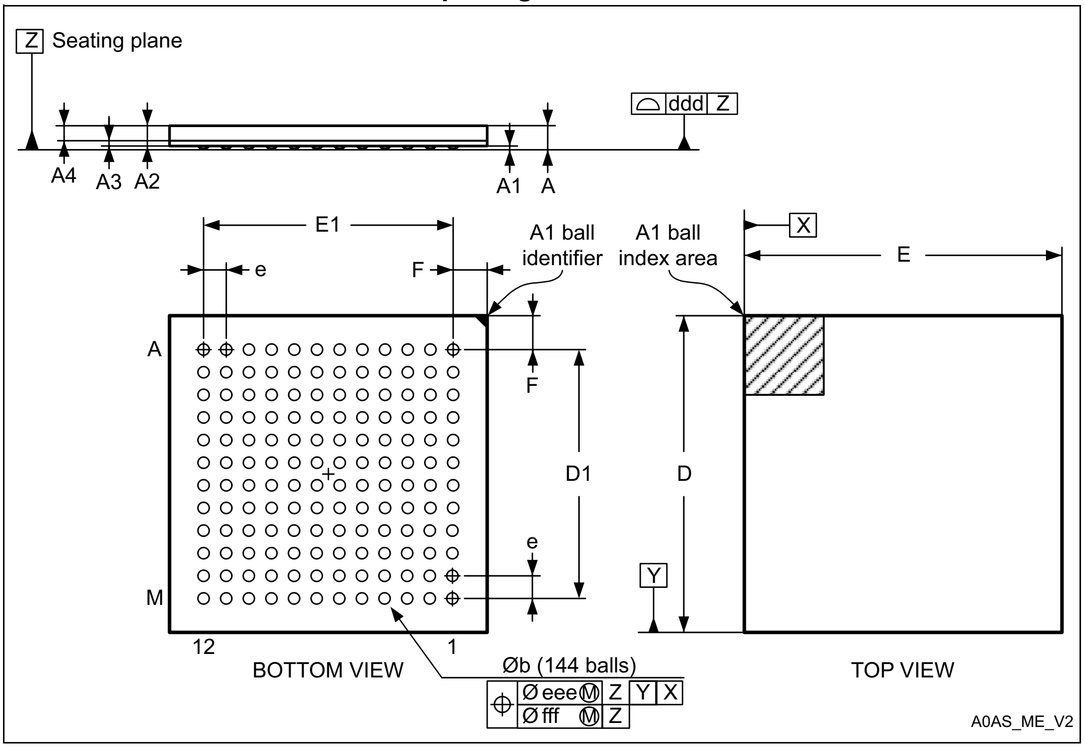
Figure 68. LQFP144 - Footprint example



1. Dimensions are expressed in millimeters.

7.5 UFBGA144 package information

Figure 69. UFBGA - 144 balls, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 125. UFBGA - 144 balls, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.230	0.280	0.320	0.0091	0.0110	0.0126
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.450	5.500	5.550	0.2146	0.2165	0.2185
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.450	5.500	5.550	0.2146	0.2165	0.2185
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315

Table 125. UFBGA - 144 balls, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 70. UFBGA - 144 balls, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

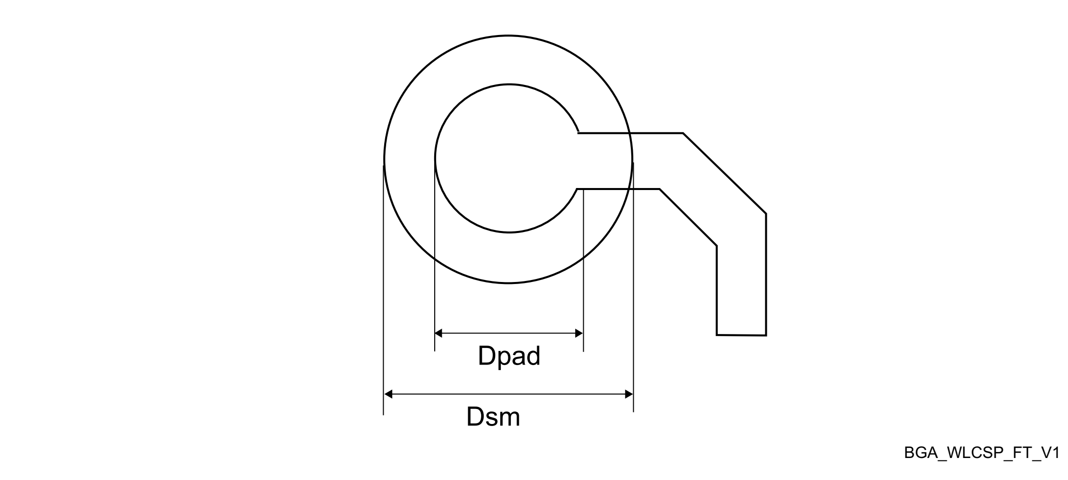


Table 126. UFBGA144 recommended PCB design rules (0.50 mm pitch BGA)

Dimension	Recommended values
Pitch	0.50 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

7.6 Thermal characteristics

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH})$,

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 127. Thermal characteristics

Symbol	Definition	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	**Thermal resistance junction-ambient** LQFP100 - 14 x 14 mm /0.5 mm pitch	43.8	°C/W
		Thermal resistance junction-ambient TFBGA100 - 8 x 8 mm /0.8 mm pitch	43.2	
		Thermal resistance junction-ambient LQFP144 - 20 x 20 mm /0.5 mm pitch	44.8	
		Thermal resistance junction-ambient UFBGA144 - 7 x 7 mm /0.5 mm pitch	36	
Θ_{JB}	Thermal resistance junction-board	**Thermal resistance junction-ambient** LQFP100 - 14 x 14 mm /0.5 mm pitch	19.8	°C/W
		Thermal resistance junction-ambient TFBGA100 - 8 x 8 mm /0.8 mm pitch	24.8	
		Thermal resistance junction-ambient LQFP144 - 20 x 20 mm /0.5 mm pitch	24.4	
		Thermal resistance junction-ambient UFBGA144 - 7 x 7 mm /0.5 mm pitch	21.1	
Θ_{JC}	Thermal resistance junction-case	**Thermal resistance junction-ambient** LQFP100 - 14 x 14 mm /0.5 mm pitch	7.3	°C/W
		Thermal resistance junction-ambient TFBGA100 - 8 x 8 mm /0.8 mm pitch	13.2	
		Thermal resistance junction-ambient LQFP144 - 20 x 20 mm /0.5 mm pitch	7.4	
		Thermal resistance junction-ambient UFBGA144 - 7 x 7 mm /0.5 mm pitch	8.7	

7.6.1 Reference documents

- JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.
- For information on thermal management, refer to application note "*Guidelines for thermal management on STM32 applications*" (AN5036) available from *www.st.com*.

8 Ordering information

Example: STM32 H 733 V G T 6 TR

Device family

STM32 = Arm-based 32-bit microcontroller

Product type

H = High performance

Device subfamily

733 = STM32H733

Pin count

V = 100 pins

Z = 144 pins

Flash memory size

G = 1024 Kbytes

Package

T = LQFP ECOPACK2

I = UFBGA pitch 0.5 mm ECOPACK2

H = TFBGA ECOPACK2

Temperature range

6 = Industrial temperature range –40 to 85 °C

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

9 Important security notice

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10 Revision history

Table 128. Document revision history

Date	Revision	Changes
10-Jul-2020	1	Initial release.
03-Sep-2020	2	Renamed *Section 3.31* into *True random number generator (RNG)*. Replaced V_{DDIOx} by V_{DD} in *Section 6: Electrical characteristics*. Updated I_{IO} in *Table 10: Current characteristics*. Updated *Table 24: Typical current consumption in Autonomous mode*, *Table 27: Typical and maximum current consumption in Standby mode* and *Table 28: Typical and maximum current consumption in VBAT mode*. Added *Section 6.3.15: I/O current injection characteristics*. Removed reference to PI8 in *Table 52: Output voltage characteristics for all I/Os except PC13, PC14 and PC15* and *Table 53: Output voltage characteristics for PC13, PC14 and PC15*. Added *Section : Analog switch between ports Pxy_C and Pxy*.
10-Dec-2021	3	Added indication that patents apply to the devices in *Section : Features*. Added reference to errata sheet in *Section 1: Introduction*. *Table 1: STM32H733xG features and peripheral counts*: – Changed number of general-purpose 32-bit timers to 4. – For LQFP100 and TFBGA100 packages, replaced 2 Octo-SPI/Quad-SPI interfaces by 1 and remove note. In *Section 3.8.1: Power supply scheme*, changed V_{DD} power supply requirements. Changed USART communication speed to 17 Mbit/s in *Section 3.37: Universal synchronous/asynchronous receiver transmitter (USART)*. *Table 7: STM32H733 pin and ball descriptions*: – Added *Note 1.* to the package pin/balls corresponding to Pxy_C. – For PA15(JTDI), replaced SPI3_NSS/I2S3_WS aternate function by SPI3_NSS(boot)/I2S3_WS. Moved LSI clock from backup domain to VDD domain in *Figure 10: Power supply scheme*. Added V_{BAT} in *Table 12: General operating conditions*. Updated *Table 15: Operating conditions at power-up/power-down* title and added t_{VCORE}. Updated measurement conditions for *Typical and maximum current consumption*. *Section : On-chip peripheral current consumption*: updated measurement conditions and *Table 29: Peripheral current consumption in Run mode*. Updated *Table 31: High-speed external user clock characteristics*. Renamed $_{ILEAK}$ parameter into I_{lkg} in *Table 51: I/O static characteristics*.

Table 128. Document revision history

Date	Revision	Changes
10-Dec-2021	3 (continued)	Updated *Table 31: High-speed external user clock characteristics*. Changed unit for PLL long-term jitter in *Table 39: PLL1 characteristics (wide VCO frequency range)*. Renamed I_{LEAK} into I_{kg} in *Table 51: I/O static characteristics* *Table 55: Output timing characteristics (HSLV ON)*: updated load capacitance condition for t_r/t_f and for speed = 10. Updated *Figure 30: OCTOSPI SDR read/write timing diagram*, *Figure 31: OCTOSPI DTR mode timing diagram*, *Figure 32: OCTOSPI Hyperbus clock timing diagram*, *Figure 33: OCTOSPI Hyperbus read timing diagram* and *Figure 34: OCTOSPI Hyperbus write timing diagram*. Updated sampling rate fro slow channels in *Table 80: 16-bit ADC characteristics*. Updated *Figure 35: ADC accuracy characteristics* and *Figure 36: Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function* as we as notes below figure. *Table 89: Temperature sensor characteristics* updated T_L max value. Changed temperature condition to 130 °C for TS_CAL2 in *Table 90: Temperature sensor calibration values*. Updated *Figure 37: Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})* Updated *Figure 44: USART timing diagram in master mode* and *Figure 45: USART timing diagram in slave mode*. Updated *Figure 54: SD high-speed mode*, *Figure 55: SD default mode* and *Figure 56: SDMMC DDR mode*. Updated *Figure 60: Ethernet MII timing diagram*. Updated *Figure 63: LQFP100 - Outline*(15), *Table 129: LQFP176 - Mechanical data*, and *Figure 72: TFBGA100 - Recommended footprint*.
16-Nov-2023	4	Updated *Figure 1: STM32H733xG block diagram*. In *Table 4: STM32H735xG features and peripheral counts*: changed the number of available Ethernet MII and SAI PDM interfaces. Updated *Section 3.39: Serial peripheral interface (SPI)/inter- integrated sound interfaces (I2S)*. Updated *Section 3.40: Serial audio interfaces (SAI)*. Added note to *Chapter 6.2*. Updated I_{IO} definition in *Table 10: Current characteristics*. Updated V_{IN} in *Table 12: General operating conditions* to cover the case of Pxy_C.

Table 128. Document revision history

Date	Revision	Changes
16-Nov-2023	4 (continued)	In *Table 16: Reset and power control block characteristics*: – renamed power-on/power-down reset threshold $V_{POR/PDR}$ into $V_{BOR0/POR/PDR}$. – updated description of $V_{hyst\_POR\_PDR}$. – renamed Hysteresis voltage for Power-on/power-down reset (including BOR0) into $V_{hyst\_POR\_PDR}$. Updated measurement conditions for *Typical and maximum current consumption* parameters. Updated *Section : High-speed external clock generated from a crystal/ceramic resonator*. Updated *Table 47: EMI characteristics for fHSE = 8 MHz and fCPU = 550 MHz*. Updated *Section : I/O static current consumption* and *Section : I/O dynamic current consumption*. Updated V_{IH} and V_{OH} in *Table 51: I/O static characteristics* and *Table 52: Output voltage characteristics for all I/Os except PC13, PC14 and PC15*, respectively, to cover the case of Pxy_C I/Os. Updated note 2 in *Table 54: Output timing characteristics (HSLV OFF)* and *Table 55: Output timing characteristics (HSLV ON)*.. Reorganized *Section 6.3.18: FMC characteristics* and updated *Figure 26: NAND controller waveforms for read access* and *Figure 27: NAND controller waveforms for write access*. Updated t_{TRIG} in *Table 82: 16-bit ADC accuracy*. Changed V_{DAC_OUT} maximum value (buffer ON) in *Table 86: DAC characteristics*. Updated $f_{DFSDMCLK}$ maximum value in *Table 98: DFSDM measured timing*. In *Table 107: USART characteristics*, changed $t_{w(SCKH)}$ and $t_{w(SCKL)}$ into $t_{w(CKH)}$ and $t_{w(CKL)}$, respectively. Updated *Figure 46: SPI timing diagram - slave mode and CPHA = 0*, *Figure 47: SPI timing diagram - slave mode and CPHA = 1* and *Figure 48: SPI timing diagram - master mode*. Updated *Figure 51: SAI master timing waveforms* and *Figure 52: SAI slave timing waveforms*. *Section : Ethernet interface characteristics*: – added constraints on Pxy_C I/Os. updated typical $t_{d(TXEN)}$ value in *Table 118: Dynamics characteristics: Ethernet MAC signals for MII*.Added *Section 7.1: Device marking*, and removed device marking sections for all packages. Updated *Table 127: Thermal characteristics* with Θ_{JA}, Θ_{JB}, and Θ_{JC} values for the UFBGA144 package. Changed SPIx_SS to SPIx_NSS in: – *Figure 1: STM32H733xG block diagram*. – *Section 3.39: Serial peripheral interface (SPI)/inter- integrated sound interfaces (I2S)*. – *Table 7: STM32H733 pin and ball descriptions*. – *Table 8: STM32H733 pin alternate functions*. – *Section : SPI interface characteristics*.